Intense PC

Hardware Specification

Legal Notice

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Revision History

Revision	Engineer	Revision Changes
1.0	Maxim Birger	Initial public release
1.1	Maxim Birger	Memory Interface updated Super-IO Controller peripheral section added RS232 serial com port info added
1.2	Maxim Birger	HDMI Block Diagram updated DP Block Diagram updated
1.3	Maxim Birger	Added power supply temperature ratings: 10.2

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1 Introduction

1.1 About This Document

This document is part of a set of reference documents providing information necessary to operate Compulab's Intense PC computer.

1.2 Reference

For additional information not covered in this manual, please refer to the documents listed in **Table 1**.

Table 1 – Reference Documents

Document	Location
FACE Module HW Specifications	http://fit-pc.com/download/face-modules/documents/face-modules-hw-specifications.pdf
Intel vPRO Technology	http://www.intel.com/content/www/us/en/architecture-and-technology/vpro/vpro-technology-general.html
Intel AMT Technology	http://www.intel.com/content/www/us/en/architecture-and-technology/intel-active-management-technology.html
Intel Virtualization Technology	http://www.intel.com/technology/virtualization/

1.3 Terms and Acronyms

Table 2 – Terms and Acronyms

Term	Definition
APM	Advanced Power Management
B2B	Board to Board (connectors)
BER	Bit error rate
bps	Bits per second
BT	Bluetooth
CAN	Controller Area Network
Codec	Coder decoder
DDR	Dual data rate
DSP	Digital signal processor
FACE Module	**F**unction **A**nd **C**onnectivity **E**xtension Module
FM-xxxx	FACE Module – *connectivity options*
GB/s	Gigabytes per second
GPIO	General-purpose input/output
GT/s	Giga Transfers per second (throughput)
HW	Hardware
JTAG	Joint Test Action Group (ANSI/ICEEE Std. 1149.1-1990)
kbps	Kilobits per second
LAN	Local Area Network
MB/s	Megabytes per second
Mbps	Megabits per second
MT/s	Mega Transfers per second (throughput)
NVM	Non Volatile Memory
OTP	One Time Programmable
PCH	Platform Controller Hub
PCM	Pulse-coded Modulation
PEG	PCI Express Graphics
Rx	Receive
SCH	System Controller Hub
SDRAM	Synchronous dynamic random access memory
SoC	System-on-Chip
SPI	Serial peripheral interface
Tx	Transmit
UART	Universal asynchronous receiver transmitter
USB	Universal serial bus
USB-OTG	Universal serial bus on-the-go
USIM	UMTS subscriber interface module
VCTCXO	Voltage-controlled temperature-compensated crystal oscillator
WLAN	Wireless Local Area Network
XO	Crystal oscillator

2 System Overview

2.1 Highlights

Intense PC is a fully functional miniature computer based on Intel 3rd generation (Ivy Bridge) Mobile Intel® Core™ 64-bit dual core processor family.

Together with powerful Intel HD graphics engine, rich peripherals and connectivity options, completely fanless design delivers outstanding performance at lowest power consumption of any PC at its class.

High performance, low-power, rich I/O and miniature rugged design, position Intense PC as an attractive solution for a wide range of applications – industrial control and automation, networking and communications infrastructures, media players, IPTV, infotainment system, digital signage and smart kiosks, gaming or small-footprint desktop replacement.

2.2 Specifications

Table 3 – Platform Specifications

Feature	Specifications
Processor	Mobile Intel® Core™ i7/5/3/Celeron 3rd Generation (Ivy Bridge)
	Dual core 64-bit
	Clock speeds 1.4GHz – 1.9GHz (turbo boost up to 2.8GHz) **(Note 1)**
	17W TDP
Chipset	Mobile Intel® QM77/HM76 Panther Point PCH
Memory	Up to 16GB (2x 8GB) DDR3-1333/1600
	2x SO-DIMM 204-pin DDR3 SDRAM memory slots
Storage	1x SATA up to 6 Gbps (SATA 3.0) for internal 2.5" HDD/SSD, HDD to be used 5400rpm only
	1x mSATA slot up to 3 Gbps (SATA 2.0)
	2x eSATA ports up to 3 Gbps (SATA 2.0)
Advanced Technologies	vPRO (On Core i7 models only)
	AMT (On Core i7 models only)
	CPU Virtualization
Operating Systems	Windows XP/7/8, 32-bit and 64-bit
	Linux 32-bit and 64-bit
	Embedded OS

Table 4 – Display and Graphics Specifications

Feature	Specifications
GPU	Intel HD Graphics 4000 Dual display mode supported
Video Output 1	HDMI 1.4a up to 1920 x 1200 @ 60Hz
Video Output 2	DisplayPort 1.1a up to 2560 x 1600 @ 60Hz

Table 5 – Audio Specifications

Feature	Specifications
Codec	Realtek ALC888-VC2 HD audio codec
Audio Output	Analog stereo output Digital 7.1+2 channels S/PDIF output 3.5mm jack
Audio Input	Analog stereo Microphone input Digital S/PDIF input 3.5mm jack

Table 6 – Networking Specifications

Feature	Specifications
LAN	2x GbE LAN ports (extendable up to 6) LAN1: Intel 82579 GbE PHY (MAC integrated into the chipset) (RJ-45) LAN2: Realtek RTL8111F-CG GbE controller (RJ-45) LAN3-6: Depends on FACE Module installed **(Note 2)**
Wireless	WLAN 802.11 b/g/n (2.4GHz Qcom Q802XRN5B module) Bluetooth 3.0 + HS

Table 7 – Connectivity Specifications

Feature	Specifications
USB	6x USB 2.0 **(Note 3)** 2x USB 3.0
Serial	1x RS232 serial communication COM1: Serial port (ultra mini serial)
Special I/O	See **Note 4**
Expansion	Half-size mini-PCIe socket Full-size mini-PCIe socket **(Note 5)**

Table 8 – Mechanical and Environmental Specifications

Feature	Specifications
Input Voltage	Unregulated 10 – 15VDC input **(Note 6)**
Power Consumption	9W – 19W (Celeron models) 10W – 26W (Core i7/5/3 models)

Operating Temperatures	1. Commercial
	   HDD models: 0°C – 50°C
	   SSD models: 0°C – 70°C
	 2. Extended (TE)
	   SSD models only: -20°C – 70°C
	 3. Industrial (TI)
	   SSD models only: -40°C – 70°C

Enclosure Material	Die Cast Aluminum
Cooling	Passive Cooling Fanless Design
Dimensions	19cm x 16cm x 4cm
Weight	1050gr

Notes:

1. For full processors specifications based on Intense PC model, please refer to models and platform SKU **Table 9**.
2. Natively 2x GbE LAN ports on the back panel with an option for additional 4x GbE LAN ports. LAN3-6 based on FACE Module installed (refer to FACE Module HW specifications - Table 1):
   a. FM-4USB: N/A
   b. FM-1LAN: LAN3 RTL8111F-CG GbE controller (RJ-45), LAN4-6: N/A
   c. FM-4LAN: Intel 82574 GbE Controller (RJ-45)
3. Back panel 2x USB2.0 and up to 4x USB2.0 on front panel based on FACE Module installed.
4. Refer to FACE Module HW specifications document - Table 1.
5. Shared with mSATA. Refer to **Figure 13**.
6. Nominal input voltage: 12V

2.3 System Block Diagram

Intense PC system Top Level Block Diagram is shown below. Later chapters in this document describe functions and entities shown in the below diagram.

Figure 1 – Intense PC Top Level Block Diagram
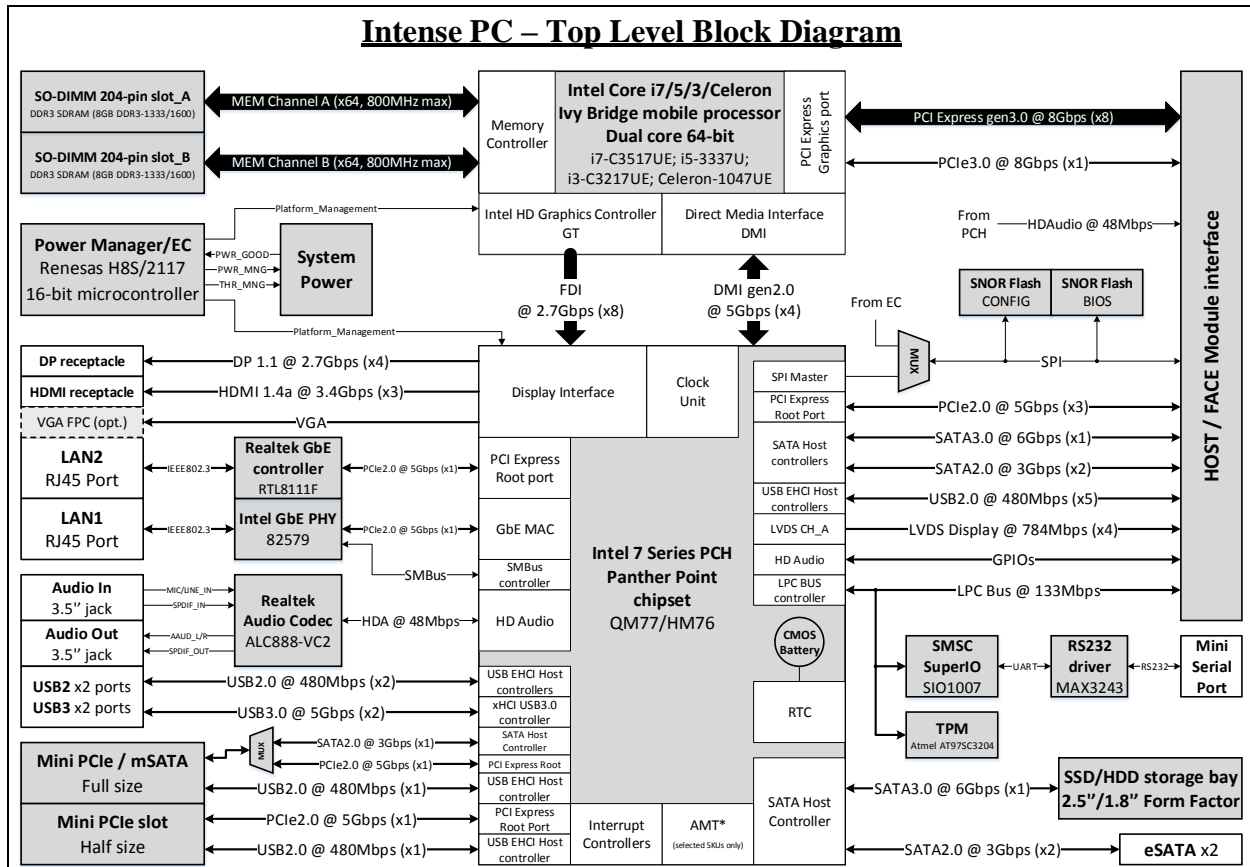
2.4 Models and Platform SKUs

Table 9 – Models and Platform SKUs

Model	Value	Business i3	Business i3 NL	Business i5	Pro
Processor	Intel Celeron 1047UE	Intel Core i3-3217UE	Intel Core i3-3227U	Intel Core i5-3337U	Intel Core i7-3517UE
Core Clock	1.4GHz	1.6GHz	1.9GHz	1.8GHz (turbo boost up to 2.7GHz)	1.7GHz (turbo boost up to 2.8GHz)
Cores	64-bit dual core	64-bit dual core	64-bit dual core	64-bit dual core	64-bit dual core
TDP	17W	17W	17W	17W	17W
Chipset	Intel HM76	Intel HM76	Intel HM76	Intel HM76	Intel QM77

3 Platform

3.1 Processor

The Mobile 3rd Generation Intel® Core™ processor family and Mobile Intel® Celeron® processor are the next generation of 64-bit, multi-core mobile processors built on 22-nanometer process technology. The processor is designed for a two-chip platform. The two-chip platform consists of a processor and a Platform Controller Hub (PCH) and enables higher performance, lower cost, easier validation, and improved x-y footprint. The processor includes Integrated Display Engine, Processor Graphics, and an Integrated Memory Controller. The processor is designed for mobile platforms.

3.1.1 Processor Features

- Two execution cores
- A 32-KB instruction and 32-KB data first-level cache (L1) for each core
- A 256-KB shared instruction / data second-level cache (L2) for each core
- Up to 8-MB shared instruction / data third-level cache (L3), shared among all cores

3.1.2 Supported Technologies

- Intel® Virtualization Technology (Intel® VT) for Directed I/O (Intel® VT-d)
- Intel® Virtualization Technology (Intel® VT) for IA-32, Intel®64 and Intel® Architecture (Intel® VT-x) Intel® Active Management Technology 8.0
- Intel® Trusted Execution Technology (Intel® TXT)
- Intel® Streaming SIMD Extensions 4.1 (Intel®SSE4.1)
- Intel® Streaming SIMD Extensions 4.2 (Intel®SSE4.2)
- Intel® Hyper-Threading Technology (Intel® HT Technology)
- Intel® 64 Architecture
- Execute Disable Bit
- Intel® Turbo Boost Technology
- Intel® Advanced Vector Extensions (Intel® AVX)
- Intel® Advanced Encryption Standard New Instructions (Intel® AES-NI)

3.2 Processor Graphics Controller

New Graphics Engine Architecture includes 3D compute elements, Multi-format hardware assisted decode/encode pipeline, and Mid-Level Cache (MLC) for superior high definition playback, video quality, and improved 3D performance and Media. The Display Engine handles delivering the pixels to the screen, and is the primary channel interface for display memory accesses and "PCI-like" traffic in and out.

3.2.1 Graphics Features

- The Processor Graphics contains a refresh of the seventh generation graphics core enabling substantial gains in performance and lower power consumption.
- Next Generation Intel Clear Video Technology HD Support is a collection of video playback and enhancement features that improve the end user's viewing experience:
  - Encode / transcode HD content
  - Playback of high definition content including Blu-ray Disc*
  - Superior image quality with sharper, more colorful images
  - Playback of Blu-ray disc S3D content using HDMI (V.1.4 with 3D)
- DirectX* Video Acceleration (DXVA) support for accelerating video processing
  - Full AVC/VC1/MPEG2 HW Decode
- Advanced Scheduler 2.0, 1.0, XPDM support
- Windows* 7, Windows* XP, Mac OSX, Linux OS Support
- DirectX* 11, DirectX* 10.1, DirectX* 10, DirectX* 9 support
- OpenGL* 3.0 support

3.3 Chipset

The PCH provides extensive I/O support. Functions and capabilities include:

- PCI Express* Base Specification, Revision 2.0 support for up to eight ports with transfers up to 5 GT/s
- PCI Local Bus Specification, Revision 2.3 support for 33 MHz PCI operations
- ACPI Power Management Logic Support, Revision 4.0a
- Enhanced DMA controller, interrupt controller, and timer functions
- Integrated SATA host controllers within dependent DMA operation on up to six ports
- USB host interface with two EHCI high-speed USB 2.0 Host controllers and two rate matching hubs provide support for up to fourteen USB 2.0 ports and one xHCI provides support for up to four SuperSpeed USB 3.0 ports.
- Integrated 10/100/1000 Gigabit Ethernet MAC with System Defense
- System Management Bus (SMBus) Specification, Version 2.0 with additional support for I2C devices
- Supports Intel® High Definition Audio (Intel® HD Audio)
- Supports Intel® Rapid Storage Technology (Intel® RST)
- Supports Intel® Active Management Technology (Intel® AMT)
- Supports Intel® Virtualization Technology for Directed I/O (Intel® VT-d)
- Integrated Clock Controller
- Intel® Flexible Display Interconnect (Intel® FDI)
- Analog and digital display interfaces
  — HDMI
  — DVI
  — DisplayPort* 1.1, Embedded DisplayPort
  — LVDS display interface
  — Analog VGA
- Low Pin Count (LPC) interface
- Serial Peripheral Interface (SPI) support
- Intel® Anti-Theft Technology (Intel® AT)

3.3.1 Chipset Capability Overview

The following sub-sections provide an overview of the PCH capabilities.

3.3.1.1 Direct Media Interface (DMI)

Direct Media Interface (DMI) is the chip-to-chip connection between the processor and PCH. This high-speed interface integrates advanced priority-based servicing allowing for concurrent traffic and true isochronous transfer capabilities. Base functionality is completely software-transparent, permitting current and legacy software to operate normally.

3.3.1.2 Flexible Display Interface (FDI)

Intel FDI connects the display engine in the processor with the display interfaces on the PCH. The display data from the frame buffer is processed by the display engine and sent to the PCH where it is transcoded and driven out on the panel. Intel FDI supports three channels – A, B, and C for

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display data transfer. Each of the Intel FDI Channel lanes uses differential signal supporting 2.7 Gbps. In case of two display configurations Intel FDI CH A maps to display pipe A while Intel CH B maps to the second display pipe B. For three display configurations, Intel FDI CH A maps to display pipe A while Intel FDI CH B divides into 2 channels - CH B and CH C of 2 lanes each, and Intel FDI CH B and C maps to display pipes B and C to send the display data from the processor to the ports.

3.3.1.3   PCH Display Interface

PCH Display Interface described in chapter 4.1.

3.3.1.4   PCI Express* Interface

The PCH provides up to 8 PCI Express Root Ports, supporting the PCI Express Base Specification, Revision 2.0. Each Root Port x1 lane supports up to 5 Gbps bandwidth in each direction (10 Gbps concurrent). PCI Express Root Ports 1–4 or Ports 5–8 can independently be configured to support four x1s, two x2s, one x2 and two x1s, or one x4 port widths.

Refer to section 5.1 for detailed feature set.

3.3.1.5   Serial ATA (SATA) Controller

The PCH has two integrated SATA host controllers that support independent DMA operation on up to six ports and supports data transfer rates of up to 6.0 Gb/s (600 MB/s) on up to two ports while all ports support rates up to 3.0 Gbps (300 MB/s) and up to 1.5 Gbps (150 MB/s). The SATA controller contains two modes of operation—a legacy mode using I/O space, and an AHCI mode using memory space. Software that uses legacy mode will not have AHCI capabilities. The PCH supports the Serial ATA Specification, Revision 3.0.

3.3.1.5.1 AHCI

The PCH provides hardware support for Advanced Host Controller Interface (AHCI), a standardized programming interface for SATA host controllers. Platforms supporting AHCI may take advantage of performance features such as no master/slave designation for SATA devices—each device is treated as a master—and hardware assisted native command queuing. AHCI also provides usability enhancements such as Hot-Plug. AHCI requires appropriate software support (such as, an AHCI driver) and for some features, hardware support in the SATA device or additional platform hardware.

3.3.1.5.2 Rapid Storage Technology

The PCH provides support for Intel Rapid Storage Technology, providing both AHCI (see above for details on AHCI) and integrated RAID functionality. The RAID capability provides high-performance RAID 0, 1, 5, and 10 functionality on up to 6 SATA ports of the PCH. Matrix RAID support is provided to allow multiple RAID levels to be combined on a single set of hard drives, such as RAID 0 and RAID 1 on two disks. Other RAID features include hot spare support, SMART alerting, and RAID 0 auto replace. Software components include an Option ROM for pre-boot configuration and boot functionality, a Microsoft Windows* compatible driver, and a user interface for configuration and management of the RAID capability of the PCH.

3.3.1.6   Low Pin Count (LPC) Interface

The PCH implements an LPC Interface as described in the LPC 1.1 Specification. The Low Pin Count (LPC) bridge function of the PCH resides in PCI Device 31: Function 0. In addition to the LPC bridge interface function, D31:F0 contains other functional units including DMA, interrupt controllers, timers, power management, system management, GPIO, and RTC.

3.3.1.7   Serial Peripheral Interface (SPI)

The PCH provides an SPI Interface and is required to be used on the platform in order to provide chipset configuration settings and Intel® ME firmware. SPI interface also used for Gigabit Ethernet MAC/PHY configuration settings implemented on the platform. The interface used as the interface for the BIOS flash device. The PCH supports up to two SPI flash devices using two chip select pins with speeds up to 50 MHz.

3.3.1.8   Universal Serial Bus (USB) Controllers

The PCH contains up to two Enhanced Host Controller Interface (EHCI) host controllers that support USB high-speed signaling. High-speed USB 2.0 allows data transfers up to 480 Mbps. The PCH supports up to fourteen USB 2.0 ports. All ports are high-speed, full-speed, and low-speed capable. The PCH also contains an integrated eXtensible Host Controller Interface (xHCI) host controller that supports up to four USB 3.0 ports. This controller allows data transfers up to 5 Gbps. The controller supports SuperSpeed (SS), high-speed (HS), full-speed (FS), and low-speed (LS) traffic on the bus.

3.3.1.9   Gigabit Ethernet Controller

Refer to section 4.2 for detailed feature set.

3.3.1.10   RTC

The PCH contains a Motorola MC146818B-compatible real-time clock with 256 bytes of battery-backed RAM. The real-time clock performs two key functions—keeping track of the time of day and storing system data, even when the system is powered down. The RTC operates on a 32.768 KHz crystal and a 3V battery.

3.3.1.11   GPIO

Various general purpose inputs and outputs are provided for custom system design. Refer to section 6.4.

3.3.1.12   System Management Bus (SMBus)

The PCH contains SMBus Host interface that allows the processor to communicate with SMBus slaves. This interface is compatible with most I2C devices. Special I2C commands are implemented.

3.3.1.13   High Definition Audio Controller

The Intel® High Definition Audio Specification defines a digital interface that can be used to attach different types of codecs, such as audio and modem codecs. The PCH Intel® HD Audio controller supports up to 4 codecs. The link can operate at either 3.3V or 1.5V. With the support of multi-channel audio stream, 32-bit sample depth, and sample rate up to 192 kHz, the Intel HD Audio

controller provides audio quality that can deliver CE levels of audio experience. On the input side, the PCH adds support for an array of microphones.

3.3.1.14 Integrated Clock Controller

The PCH contains a Fully Integrated Clock Controller (ICC) generating various platform clocks from a 25 MHz crystal source. The ICC contains up to eight PLLs and four Spread Modulators for generating various clocks suited to the platform needs. The ICC supplies up to ten 100 MHz PCI Express 2.0 Specification compliant clocks, one 100 MHz BCLK/DMI to the processor, one 120 MHz for embedded DisplayPort on the processor, four 33 MHz clocks for SIO/EC/LPC/TPM devices and four Flex Clocks that can be configured to various frequencies that include 14.318 MHz, 27 MHz, 33 MHz and 24/48 MHz for use with SIO, EC, LPC, and discrete Graphics devices.

3.4 System Memory

3.4.1 Processor Integrated Memory Controller

Processor's Integrated Memory Controller (IMC) supports DDR3 / DDR3L / DDR3L-RS protocols with two independent, 64-bit wide channels, each accessing one or two DIMMs. The IMC supports one or two, unbuffered non-ECC DDR3 DIMM per-channel; thus, allowing up to four device ranks per-channel.

Figure 2 – Memory Interface
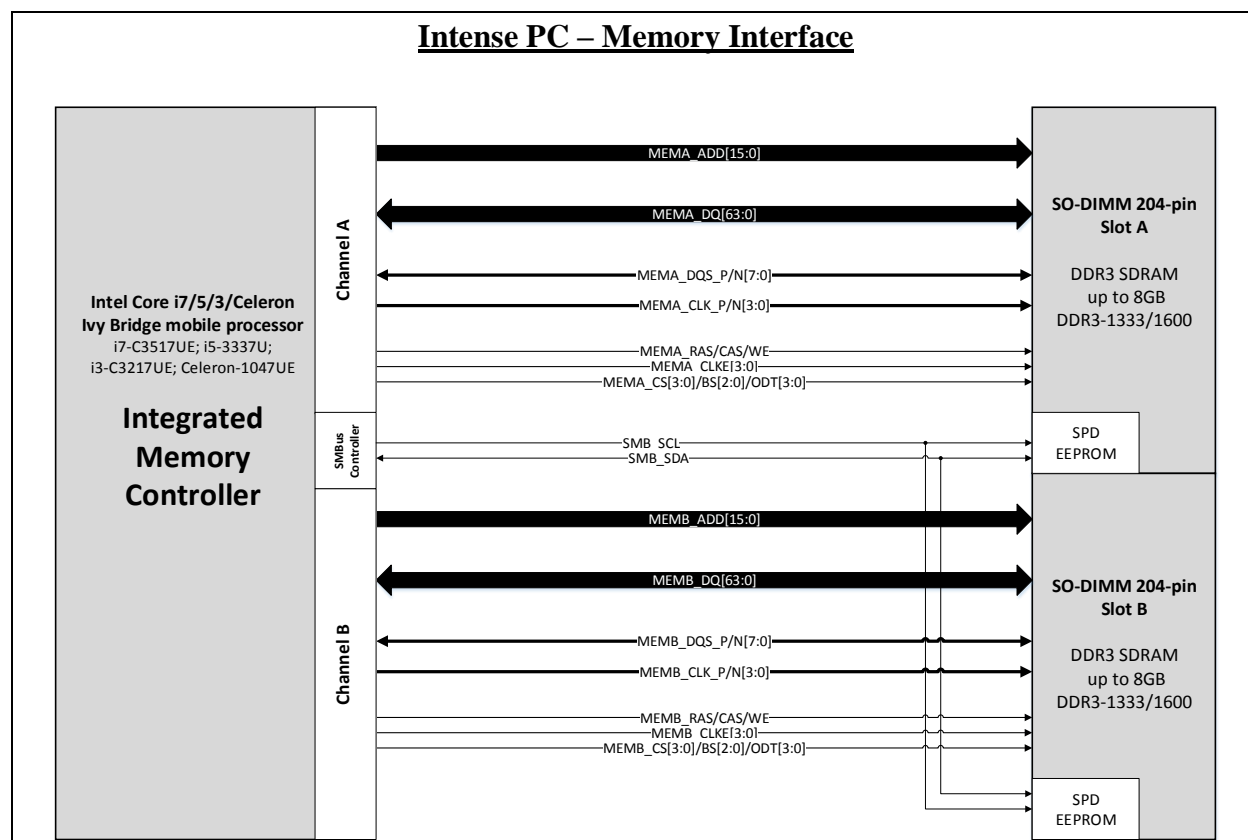
3.4.2 System Supported Memory

- Two channels of DDR3 SDRAM memory with unbuffered Small Outline Dual In-Line Memory 204-pin Modules (SO-DIMM)
- Up to 16GB (2x 8GB) DDR3-1333/1600
- Single-channel and dual-channel memory organization modes
- Data burst length of eight for all memory organization modes
- System Memory Interface I/O Voltage of 1.5 V only
- DDR3 SDRAM SO-DIMMs running at 1.5 V only
- 64-bit wide channels
- Non-ECC, Unbuffered DDR3 SO-DIMMs only
- Theoretical maximum memory bandwidth of:
  - — 21.3 GB/s in dual-channel mode assuming DDR3 SDRAM 1333 MT/s
  - — 25.6 GB/s in dual-channel mode assuming DDR3 SDRAM 1600 MT/s
- 1Gb, 2Gb, and 4Gb DDR3 SDRAM device technologies are supported
  - — Standard 1-Gb, 2-Gb, and 4-Gb technologies and addressing are supported for x16 and x8 devices. There is no support for memory modules with different technologies or capacities on opposite sides of the same memory module. If one side of a memory module is populated, the other side is either identical or empty.
- On-Die Termination (ODT)

Table 10 – Supported Memory Technologies

Raw Card Version	DIMM Capacity	DRAM Device Technology	DRAM Organization	# of DRAM Devices	# of Physical Device Ranks	# of Row/Col Address Bits	# of Banks Inside DRAM	Page Size
A	2 GB	2 Gb	128 M x 16	8	2	14/10	8	8K
	4 GB	4 Gb	256 M x 16	8	2	15/10	8	8K
B	1 GB	1 Gb	128 M x 8	8	1	14/10	8	8K
	2 GB	2 Gb	256 M x 8	8	1	15/10	8	8K
	4 GB	4 Gb	512 M x 8	8	1	16/10	8	8K
C	1 GB	2 Gb	128 M x 16	4	1	14/10	8	8K
	2 GB	4 Gb	256 M x 16	4	1	15/10	8	8K
F	2 GB	1 Gb	128 M x 8	16	2	14/10	8	8K
	4 GB	2 Gb	256 M x 8	16	2	15/10	8	8K
	8 GB	4 Gb	512 M x 8	16	2	16/ 10	8	8K

Table 11 – Supported Max Memory Size per SO-DIMM

Platform	Package	Memory	Max Size per DIMM [GB]
Mobile	rPGA	SODIMM RC A	4
		SODIMM RC B	4
		SODIMM RC C	2
		SODIMM RC F	8

3.4.3 System Memory Timing Support

The IMC supports the following Speed Bins, CAS Write Latency (CWL), and command signal mode timings on the main memory interface:

- tCL = CAS Latency
- tRCD = Activate Command to READ or WRITE Command delay
- tRP = PRECHARGE Command Period
- CWL = CAS Write Latency
- Command Signal modes = 1N indicates a new command may be issued every clock and 2N indicates a new command may be issued every 2 clocks. Command launch mode programming depends on the transfer rate and memory configuration.

Table 12 – DDR3 System Memory Timing Support

Segment	Transfer Rate (MT/s)	tCL (tCK)	tRCD (tCK)	tRP (tCK)	CWL (tCK)	DPC	CMD Mode
Dual Core Standard Voltage (SV)	1066	7	7	7	6	1	1N/2N
		8	8	8	6	1	1N/2N
	1333	9	9	9	7	1	1N/2N
	1600	11	11	11	8	1	1N/2N

3.4.4 System Memory Organization Modes

The IMC supports two memory organization modes, single-channel and dual-channel. Depending upon how the SO-DIMM Modules are populated in each memory channel, a number of different configurations can exist.

3.4.4.1 Single-Channel Mode

In this mode, all memory cycles are directed to a single-channel. Single-channel mode is used when either Channel A or Channel B SO-DIMM connectors are populated in any order, but not both.

3.4.4.2 Dual-Channel Mode (Intel Flex Memory Technology Mode)

The IMC supports Intel Flex Memory Technology Mode. Memory is divided into a symmetric and asymmetric zone. The symmetric zone starts at the lowest address in each channel and is contiguous until the asymmetric zone begins or until the top address of the channel with the smaller capacity is reached. In this mode, the system runs with one zone of dual-channel mode and one zone of single-channel mode, simultaneously, across the whole memory array.

Note: Channels A and B can be mapped for physical channel 0 and 1 respectively or vice versa; however, channel A size must be greater or equal to channel B size.

3.4.4.3 Dual-Channel Symmetric Mode

Dual-Channel Symmetric mode, also known as interleaved mode, provides maximum performance on real world applications. Addresses are ping-ponged between the channels after each cache line (64-byte boundary). If there are two requests, and the second request is to an address on the opposite channel from the first, that request can be sent before data from the first request has returned. If two consecutive cache lines are requested, both may be retrieved simultaneously, since they are ensured to be on opposite channels. Use Dual-Channel Symmetric mode when both Channel A and Channel B SO-DIMM connectors are populated in any order, with the total amount of memory in each channel being the same. When both channels are populated with the same memory capacity and the boundary between the dual channel zone and the single channel zone is the top of memory, IMC operates completely in Dual-Channel Symmetric mode.

Note: The DRAM device technology and width may vary from one channel to the other.

3.4.4.4 Rules for Populating Memory Slots

In all System Memory Organization Modes, the frequency and latency timings of the system memory is the lowest supported frequency and slowest supported latency timings of all memory DIMM modules placed in the system.

3.5   Storage

Intense PC supports various types of storage devices due to advanced PCH SATA Host Controller capabilities and I/O availability, described in section 3.3.1.5. Supported devices include HDD and SSD storage devices in 2.5'' form factor. HDD limited to 5400rpm only due to power dissipation reasons. mSATA NAND Flash solid state drive modules supported as well and share mini PCIe full size slot. For detailed architecture refer to section 6.1 .

In addition, Intense PC offers two eSATA connectors, available on the back panel which allow connection of external storage drives. Intense PC storage architecture and BIOS features RAID functionality. Note eSATA connectivity provide signaling only, when power to the external drives must be supplied externally.

Figure 3 – SATA Interface
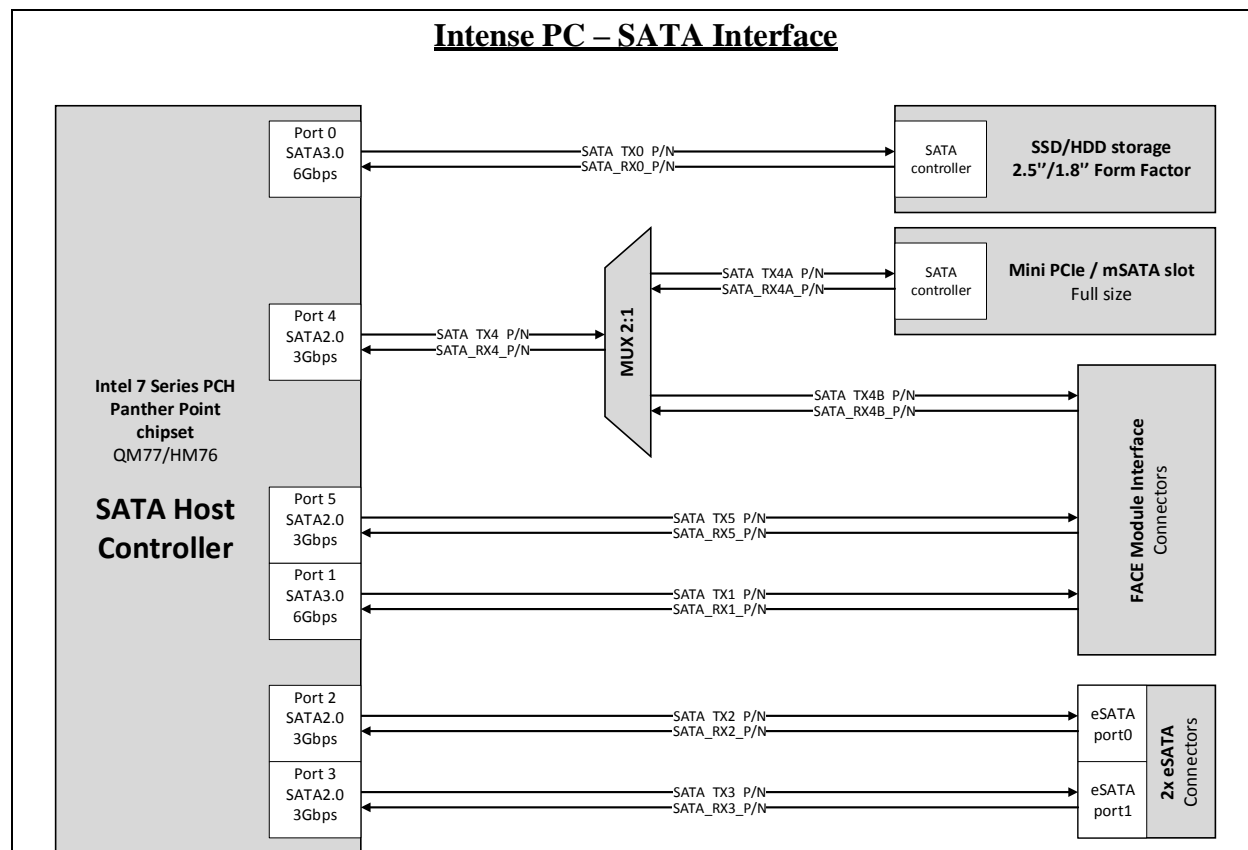
3.5.1 Certified storage devices

3.5.1.1 HDD examples

Table 13 – WD Scorpio Blue HDD series

Specifications	1 TB	1 TB	750 GB	750 GB	500 GB
Model number	WD10SPCX	WD10JPVX WD10JPVT	WD7500LPCX	WD7500BPVX WD7500BPVT	WD5000LPVX WD5000LPVT
Interface	SATA 6 Gb/s	SATA 6 Gb/s (JPVX) SATA 3 Gb/s (JPVT)	SATA 6 Gb/s	SATA 6 Gb/s (BPVX) SATA 3 Gb/s (BPVT)	SATA 6 Gb/s (LPVX) SATA 3 Gb/s (LPVT)
Formatted capacity[1]	1,000,204 MB	1,000,204 MB	750,156 MB	750,156 MB	500,107 MB
User sectors per drive	1,953,525,168	1,953,525,168	1,465,149,168	1,465,149,168	976,773,168
Advanced Format (AF)	Yes	Yes	Yes	Yes	Yes
Form factor	2.5-inch	2.5-inch	2.5-inch	2.5-inch	2.5-inch
RoHS compliant[2]	Yes	Yes	Yes	Yes	Yes
Performance					
Data transfer rates Interface speed	6 Gb/s	6 Gb/s (JPVX) 3 Gb/s (JPVT)	6 Gb/s	6 Gb/s (BPVX) 3 Gb/s (BPVT)	6 Gb/s (LPVX) 3 Gb/s (LPVT)
Internal transfer rate (max)	140 MB/s	144 MB/s	140 MB/s	138 MB/s	147 MB/s
Cache (MB)	16	8	16	8	8
Average latency (ms)	5.5	5.5	5.5	5.5	5.5
Rotational speed (RPM)	5400	5400	5400	5400	5400
Average drive ready time (sec)	2.8	3.0 (JPVX) / <3.5 (JPVT)	2.8	3.0 (BPVX) / 4.0 (BPVT)	2.8 (LPVX) / <3.5 (LPVT)
Reliability/Data Integrity					
Load/unload cycles[3]	600,000	600,000	600,000	600,000	600,000
Non-recoverable read errors per bits read	<1 in 10^{14}	<1 in 10^{14}	<1 in 10^{14}	<1 in 10^{14}	<1 in 10^{14}
Limited warranty (years)[4]	2	2	2	2	2
Power Management					
5VDC ±10% (A, peak)	1.00	1.00 (JPVX) / 0.900 (JPVT)	1.00	1.00 (BPVX) / 0.975 (BPVT)	1.00 (LPVX) / 0.900 (LPVT)

Average power requirements (W)
  Read/Write
  Idle
  Standby/Sleep
	1.7
	0.57
	0.18
		1.4
		0.59
		0.18
			1.7
			0.57
			0.18
				1.6
				0.65
				0.20
					1.4
					0.55
					0.13

Environmental Specifications[5]					

Temperature (°C)
  Operating
  Non-operating
	0 to 60
	-40 to 65
		0 to 60
		-40 to 65
			0 to 60
			-40 to 65
				0 to 60
				-40 to 65
					0 to 60
					-40 to 65

Shock (Gs)
  Operating (2 ms, read)
  Non-operating
	350
	1000 (2 ms)
		400
		1000 (2 ms)
			350
			1000 (2 ms)
				350
				1000 (2 ms)
					400
					1000 (2 ms)

Acoustics (dBA)[6]
  Idle
  Seek (average)
	20
	21
		24
		25
			20
			21
				24
				25
					17
					22

Physical Dimensions					
Height (in./mm, max)	0.28/7.0	0.374/9.50	0.28/7.0	0.374/9.50	0.28/7.0
Length (in./mm, max)	3.94/100.20	3.94/100.20	3.94/100.20	3.94/100.20	3.94/100.20
Width (in./mm, ± .01 in.)	2.75/69.85	2.75/69.85	2.75/69.85	2.75/69.85	2.75/69.85
Weight (lb./kg, ± 10%)	0.21/0.09	0.27/0.12	0.21/0.09	0.34/0.15	0.20/0.09

Table 14 – WD Scorpio Blue HDD series (cont.)

Specifications	500 GB	500 GB	320 GB	320 GB	250 GB	250 GB
Model number	WD5000MPCK	WD5000BPVT	WD3200LPVX WD3200LPVT	WD3200BPVT	WD2500LPVX WD2500LPVT	WD2500BPVT
Interface	SATA 6 Gb/s	SATA 3 Gb/s	SATA 6 Gb/s (LPVX) SATA 3 Gb/s (LPVT)	SATA 3 Gb/s	SATA 6 Gb/s (LPVX) SATA 3 Gb/s (LPVT)	SATA 3 Gb/s
Formatted capacity[1]	500,107 MB	500,107 MB	320,072 MB	320,072 MB	250,059 MB	250,059 MB
User sectors per drive	976,773,168	976,773,168	625,142,448	625,142,448	488,397,168	488,397,168
Advanced Format (AF)	Yes	Yes	Yes	Yes	Yes	Yes
Form factor	2.5-inch	2.5-inch	2.5-inch	2.5-inch	2.5-inch	2.5-inch
RoHS compliant[2]	Yes	Yes	Yes	Yes	Yes	Yes
Performance						
Data transfer rates						
Interface speed	6 Gb/s	3 Gb/s	6 Gb/s (LPVX) 3 Gb/s (LPVT)	3 Gb/s	6 Gb/s (LPVX) 3 Gb/s (LPVT)	3 Gb/s
Internal transfer rate (max)	145 MB/s	136 MB/s	147 MB/s (LPVX) 109 MB/s (LPVT)	116 MB/s	147 MB/s (LPVX) 109 MB/s (LPVT)	116 MB/s
Cache (MB)	16	8	8	8	8	8
Average latency (ms)	5.5	5.5	5.5	5.5	5.5	5.5
Rotational speed (RPM)	5400	5400	5400	5400	5400	5400
Average drive ready time (sec)	2.8	4.0	2.8 (LPVX) / <3.5 (LPVT)	4.0	2.8 (LPVX) / <3.5 (LPVT)	4.0
Reliability/Data Integrity						
Load/unload cycles[3]	600,000	600,000	600,000	600,000	600,000	600,000
Non-recoverable read errors per bits read	<1 in 10^{14}	<1 in 10^{14}	<1 in 10^{14}	<1 in 10^{14}	<1 in 10^{14}	<1 in 10^{14}
Limited warranty (years)[4]	2	2	2	2	2	2
Power Management						
5VDC ±10% (A, peak)	0.900	0.950	1.00 (LPVX) / 0.900 (LPVT)	1.00	1.00 (LPVX) / 0.900 (LPVT)	1.00
Average power requirements (W)						
Read/Write	1.5	1.6	1.4	2.5	1.4	2.5
Idle	0.55	0.65	0.55	0.85	0.55	0.85
Standby/Sleep	0.15	0.20	0.13	0.20	0.13	0.20
Environmental Specifications[5]						
Temperature (°C)						
Operating	0 to 60	0 to 60	0 to 60	0 to 60	0 to 60	0 to 60
Non-operating	-40 to 65	-40 to 65	-40 to 65	-40 to 65	-40 to 65	-40 to 65
Shock (Gs)						
Operating (2 ms, read)	400	350	400	350	400	350
Non-operating	1000 (2 ms)	1000 (2 ms)	1000 (2 ms)	1000 (2 ms)	1000 (2 ms)	1000 (2 ms)
Acoustics (dBA)[6]						
Idle	15	22	17	22	17	22
Seek (average)	17	25	22	25	22	25
Physical Dimensions						
Height (in./mm, max)	0.20/5.0	0.374/9.50	0.28/7.0	0.374/9.50	0.28/7.0	0.374/9.50
Length (in./mm, max)	3.95/100.30	3.94/100.20	3.94/100.20	3.94/100.20	3.94/100.20	3.94/100.20
Width (in./mm, ± .01 in.)	2.75/69.85	2.75/69.85	2.75/69.85	2.75/69.85	2.75/69.85	2.75/69.85
Weight (lb./kg, ± 10%)	0.16/0.07	0.22/0.10	0.20/0.09	0.22/0.10	0.20/0.09	0.22/0.10

Table 15 – Hitachi CinemaStar C5K750 HDD models

Model(s)	HCC547575A9E380 HCC547564A9E380 HCC547550A9E380
Configuration	
Interface	SATA 3Gb/s
Capacity (GB)[1]	750 / 640 / 500
Sector size (bytes)[2]	512e
Recording zones	24
Max. areal density (Gbits/sq. in.)	492
Performance	
Data buffer (MB)[3]	8
Rotational speed (RPM)	5400
Latency average (ms)	5.5
Media transfer rate (Mbits/sec, max.)	996
Interface transfer rate (MB/sec, max.)	300
Seek time, read (ms, typical)[4]	15
Reliability	
Load/unload cycles	600,000
Power on Hours (POH) per month	730
Availability[5] (hrs/day x days/wk)	24x7
Power	
Requirement	+5 VDC (+/-5%)
Startup (W, peak, max.)	3.5
Operating[6] (W, avg.)	1.5
Low power idle (W, avg.)	0.5
Physical size	
z-height (mm)	9.5
Dimensions (width x depth, mm)	70 x 100
Weight (g, typical)	102
Environmental (operating)	
Shock (half-sine wave)	400G (2ms), 225G (1ms)
Operating temperature[7]	0º to 70ºC
Environmental (non-operating)	
Shock (half-sine wave)	1000G (1ms)
Ambient temperature	-40º to 65ºC
Acoustics (A-weighted sound power)	
Idle (Bels, typical)	2.4
Seek (Bels, typical)	2.5

Table 16 – Seagate Momentus HDD series

Seagate® Momentus® 2.5" Internal Drive
Instant Add-on Storage

Interface SATA
Capacities 250GB, 320GB, 500GB, 640GB, 750GB

Momentus LP Drive – Energy Efficient, High Capacity Storage

Engineered specifically for low-power applications, the Momentus LP internal drive has a 5400RPM spindle speed and a 8MB cache to provide energy-efficient performance at whisper-quiet acoustic levels. With reduced power consumption and heat generation, this drive will reduce power costs up to 50% over the life of the system compared to standard drives. It is optimized for standard laptops and small form factor PCs.
• 5400RPM
• 8MB cache
• SATA 3Gb/s interface with Native Command Queueing
• QuietStep™ technology enables ultra-quiet load/unload acoustics
• Perpendicular recording technology increases performance and reliability

3.5.1.2 mSATA SSD examples

Table 17 – Micron mSATA NAND Flash SSD

Micron

M500 mSATA NAND Flash SSD
Features

M500 mSATA NAND Flash SSD

MTFDDAT120MAV, MTFDDAT240MAV, MTFDDAT480MAV

Features

- Micron® 20nm MLC NAND Flash
- RoHS-compliant package
- SATA 6 Gb/s interface
- TCG/Opal 2.0-compliant self-encrypting drive (SED)
- Hardware-based AES-256 encryption engine
- ATA modes supported
  - PIO mode 3, 4
  - Multiword DMA mode 0, 1, 2
  - Ultra DMA mode 0, 1, 2, 3, 4, 5
- Industry-standard, 512-byte sector size support
- Device Sleep (DEVSLP), extreme low power mode
- Native command queuing support with 32-command slot support
- ATA-8 ACS2 command set compliant
- ATA security feature command set and password login support
- Secure erase (data page) command set: fast and secure erase
- Sanitize device feature set support
- Self-monitoring, analysis, and reporting technology (SMART) command set
- Windows 8 drive telemetry
- Adaptive thermal monitoring
- Performance[1, 2]
  - PCMark® Vantage (HDD test suite score): up to 80,000
  - Sequential 128KB READ: up to 500 MB/s
  - Sequential 128KB WRITE: up to 400 MB/s
  - Random 4KB READ: up to 80,000 IOPS
  - Random 4KB WRITE: up to 80,000 IOPS
  - READ/WRITE latency: 5ms/25ms (MAX)

- Reliability
  - MTTF: 1.2 million device hours[3]
  - Static and dynamic wear leveling
  - Uncorrectable bit error rate (UBER): <1 sector per 10^{15} bits read
- Low power consumption
  - 150mW TYP[4]
- Endurance: Total bytes written (TBW) – 72TB
- Capacity[5] (unformatted): 120GB, 240GB, 480GB
- Mechanical
  - mSATA connector: 3.3V ±5%
  - Caseless design: 50.80mm x 29.85mm x 3.75mm
  - Weight: 10g (MAX)
- Secure firmware update with digitally signed firmware image
- Operating temperature
  - Commercial (0°C to +70°C)[6]

Notes:
1. Typical I/O performance numbers as measured fresh-out-of-box (FOB) using Iometer with a queue depth of 32 and write cache enabled.
2. 4KB transfers used for READ/WRITE latency values.
3. The product achieves a mean time to failure (MTTF) based on population statistics not relevant to individual units.
4. Active average power measured during execution of MobileMark® with DIPM (device-initiated power management) enabled.
5. 1GB = 1 billion bytes; formatted capacity is less.
6. Drive on-board sensor temperature.

Warranty: Contact your Micron sales representative for further information regarding the product, including product warranties.

Table 18 – ACPI CMS2G-M SSD

Specification	
Model Name	CMS2G-M
Interface	SATA III 6Gb/s compatible
NAND Flash Type	MLC
Connector Type	miniPCIe mSATA
External DRAM Buffer	Yes
Capacity	32GB~256GB
Sequential R/W (128KB, Typ.)	Max 530/330 MB/s
Random R/W (4KB, Typ.)	Max 94K/75K IOPS
Temperature	Operating Temp.:0˚C~+70˚C Storage Temp.: -40˚C~+90˚C
TRIM	Support
S.M.A.R.T. (Health Monitor)	Support
Security Tool	-
MTBF	> 1.2 million hours
Vibration (Operating)	20G Peak, 7~2000Hz
Shock	1500G, 0.5ms
Dimension (LxWxH)	50.8*29.85*3.7mm
Weight	8 gram
Warranty	3 Year

4 Peripherals

4.1 Display Interface

Display is divided between processor and PCH. The processor houses memory interface, display planes, and pipes while PCH has transcoder and display interface or ports. Intel® FDI connects the processor and PCH display engine. The number of planes, pipes, and transcoders decide the number of simultaneous and concurrent display devices that can be driven on a platform. PCH will continue to support single display and two simultaneous and concurrent legacy display configurations. The PCH integrates one Analog, LVDS and three Digital Ports B, C, and D. Each Digital Port can transmit data according to one or more protocols. Digital Port B, C, and D can be configured to drive natively HDMI, DisplayPort*, or DVI. Each digital port has control signals that may be used to control, configure and/or determine the capabilities of an external device. Intense PC design supports one, two or three simultaneous independent and concurrent display configurations, when two displays supported natively and for additional 3rd display provision is given.

The Processor Graphics controller display pipe can be broken down into three components:

- Display Planes
- Display Pipes
- Embedded DisplayPort* and Intel® FDI

Processor and PCH display data path architecture described in *Figure 4* and *Figure 5*.
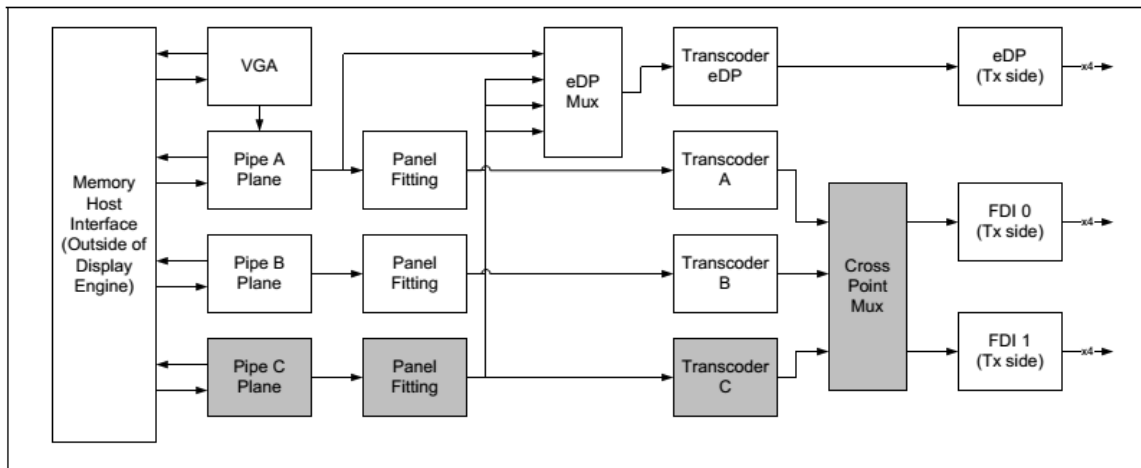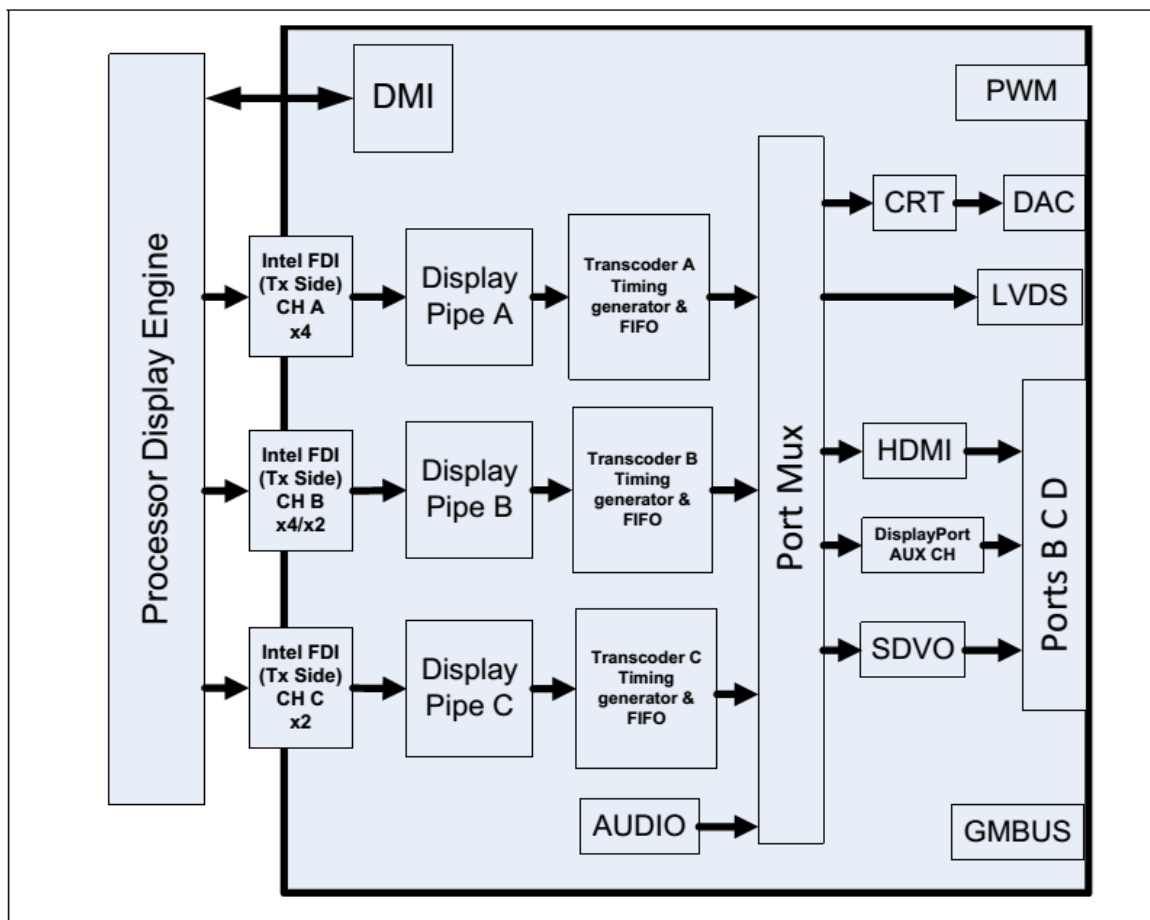
Figure 4 – Processor Display Architecture

Figure 5 – PCH Display Architecture

4.2   Network

The following section provides information about Intense PC main network components and features.

4.2.1   LAN1 – Intel MAC/PHY GbE Controller

The PCH integrates a Gigabit Ethernet (GbE) controller. The integrated GbE controller is compatible with the Intel® 82579 Platform LAN PHY device. The integrated GbE controller provides two interfaces for 10/100/1000 Mbps and manageability operation:

- Based on PCI Express – A high-speed SerDes interface using PCI Express electrical signaling at half speed while keeping the custom logical protocol for active state operation mode.
- System Management Bus (SMBus) – A very low speed connection for low power state mode for manageability communication only. At this low power state mode the Ethernet link speed is reduced to 10 Mbps.

The 82579 can be connected to any available PCI Express port in the PCH. The 82579 only runs at a speed of 1250 Mbps, which is 1/2 of the 2.5 Gbps PCI Express frequency. Each of the PCI Express root ports in the PCH have the ability to run at the 1250 Mbps rate. There is no need to implement a mechanism to detect that the 82579 LAN device is connected. The port configuration (if any), attached to the 82579 LAN device, is preloaded from the NVM. The selected port adjusts the transmitter to run at the 1250 Mbps rate and does not need to be PCI Express compliant.

The integrated GbE controller operates at full-duplex at all supported speeds or half duplex at 10/100 Mbps. It also adheres to the IEEE 802.3x Flow Control Specification. GbE operation (1000 Mbps) is only supported in S0 mode. In Sx modes, SMBus is the only active bus and is used to support manageability/remote wake-up functionality. The integrated GbE controller provides a system interface using a PCI Express function. A full memory-mapped or I/O-mapped interface is provided to the software, along with DMA mechanisms for high performance data transfer.

The integrated GbE controller features are:

- Network Features
  - Compliant with the 1 Gbps Ethernet 802.3 802.3u 802.3ab specifications
  - Multi-speed operation: 10/100/1000 Mbps
  - Full-duplex operation at 10/100/1000 Mbps: Half-duplex at 10/100 Mbps
  - Flow control support compliant with the 802.3X specification
  - VLAN support compliant with the 802.3q specification
  - MAC address filters: perfect match unicast filters; multicast hash filtering, broadcast filter and promiscuous mode
  - PCI Express/SMBus interface to GbE PHYs

- Performance Features
  - Configurable receive and transmit data FIFO, programmable in 1 KB increments
  - TCP segmentation capability compatible with Windows NT* 5.x offloading features

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- — Fragmented UDP checksum offload for packet reassembly
- — IPv4 and IPv6 checksum offload support (receive, transmit, and TCP segmentation offload)
- — Split header support to eliminate payload copy from user space to host space
- — Receive Side Scaling (RSS) with two hardware receive queues
- — Supports 9018 bytes of jumbo packets
- — Packet buffer size
- — LinkSec offload compliant with 802.3ae specification
- — TimeSync offload compliant with 802.1as specification

- ▪ Power Management Features
  - — Magic Packet* wake-up enable with unique MAC address
  - — ACPI register set and power down functionality supporting D0 and D3 states
  - — Full wake up support (APM, ACPI)
  - — MAC power down at Sx, DMoff with and without WoL

4.2.2 LAN2 – Realtek RTL8111F GbE Controller

The Realtek RTL8111F Gigabit Ethernet controller combines a triple-speed IEEE 802.3 compliant Media Access Controller (MAC) with a triple-speed Ethernet transceiver, PCI Express bus controller, and embedded memory. With state-of-the-art DSP technology and mixed-mode signal technology, the RTL8111F offers high-speed transmission over CAT 5 UTP cable.

The RTL8111F supports PCI Express 1.1 bus interface for host communications with power management, and is compliant with the IEEE 802.3u specification for 10/100Mbps Ethernet and the IEEE 802.3ab specification for 1000Mbps Ethernet. It also supports an auxiliary power auto-detect function, and will auto-configure related bits of the PCI power management registers in PCI configuration space. The RTL8111F features embedded One-Time-Programmable (OTP) memory to replace the external EEPROM.

Advanced Configuration Power management Interface (ACPI) – power management for modern operating systems that are capable of Operating System-directed Power Management (OSPM) – is supported to achieve the most efficient power management possible. In addition to the ACPI feature, remote Wake on LAN is supported in both ACPI and APM (Advanced Power Management) environments.

The RTL8111F is suitable for multiple market segments and emerging applications, such as desktop, mobile, workstation, server, communications platforms and embedded applications.

4.2.2.1 Realtek RTL8111F Features

Realtek RTL8111F Gigabit Ethernet controller main features show below:

- ▪ Integrated 10/100/1000 transceiver
- ▪ Auto-Negotiation with Next Page capability
- ▪ Supports PCI Express 1.1

- Supports pair swap/polarity/skew correction
- Crossover Detection & Auto-Correction
- Wake-on-LAN and remote wake-up support
- Supports Full Duplex flow control (IEEE 802.3x)
- Supports jumbo frame to 9K bytes
- Fully compliant with IEEE 802.3, IEEE 802.3u, IEEE 802.3ab
- Supports IEEE 802.1P Layer 2 Priority Encoding
- Supports IEEE 802.1Q VLAN tagging
- Supports IEEE 802.3az-2010 (EEE)
- Embedded OTP memory can replace the external EEPROM
- Supports power down/link down power saving/PHY disable mode
- Built-in switching regulator
- Supports Customized LEDs
- Supports 1-Lane 2.5Gbps PCI Express Bus
- Supports hardware ECC (Error Correction Code) function
- Supports hardware CRC (Cyclic Redundancy Check) function

4.2.3 LAN Ports LEDs notifications

LAN ports LEDs status notifications shown in the table below:

Table 19 – LAN ports LEDs status notification

LED color	Mode	Function
Yellow	Blink	Activity
Green	On	100 Mbps
	Off	10/1000 Mbps

4.3 Wireless Networks

Intense PC current official WLAN + Bluetooth module is Qcom's Q802XRN5B, in a mini PCIe half size form factor. The Q802XRN5B is highly integrated 2.4GHz single band IEEE 802.11b/g/n and Bluetooth 3.0, in a single Realtek RTL8723AE chip with a single PCI-E interface. The integration enhances coordination between 802.11 and Bluetooth, with dynamic power control reducing power consumption, and packet traffic arbitration offering coexistence performance unattainable by two chip solutions.

Note: Any other mini PCIe half size RF module can be installed and with relevant driver package can provide wireless infrastructure for the system. Q802XRN5B module uses single PCIe as Host interface for both WLAN and BT communication.

Modules with **2** Host interfaces can be used as well, when PCI Express Host interface used for communication with WLAN part of a baseband chip and USB Host interface used for communication with BT part of a baseband chip.

4.4 Wireless Module Features

- Realtek RTL8723AE WLAN + BT
- One Transmit and one Receive path (1T1R)
- 20MHz and 40MHz bandwidth transmission
- Compatible with 802.11n specification
- 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services
- IEEE 802.11b/g/n compatible WLAN
- IEEE 802.11e QoS Enhancement (WMM)
- IEEE 802.11h TPC, Spectrum Measurement
- Short Guard Interval (400ns)
- DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble
- Bluetooth 3.0+HS/2.1+EDR Compliant
- Bluetooth Low Energy supported
- Enhanced BT/WIFI Coexistence Control to improve transmission quality in different profiles

Figure 6 – Wireless Module Q802XRN5B Block Diagram
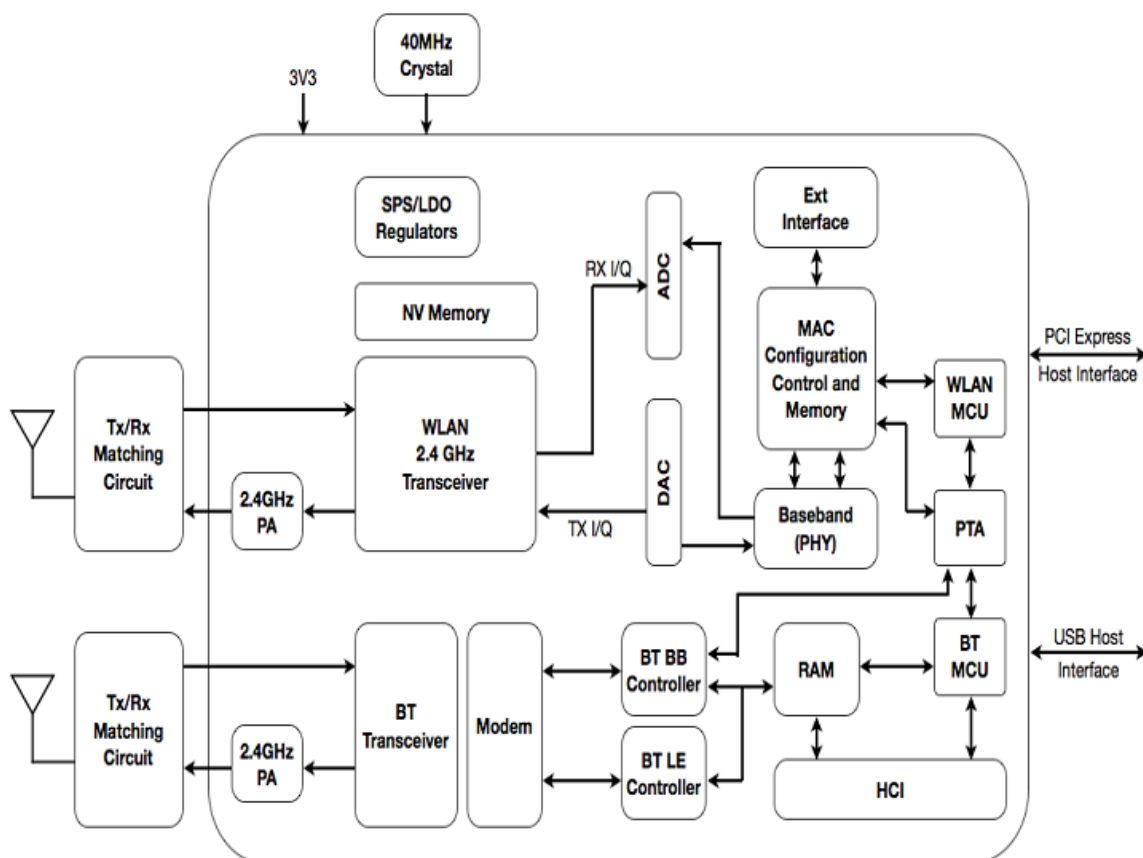
4.4.1 WLAN

Figure 7 – WLAN Channel Assignment

Channel	Frequency	FCC (US)	IC (CA)	ETSI (EU)	Japan (JP)
1	2412MHz	V	V	V	V
2	2417MHz	V	V	V	V
3	2422MHz	V	V	V	V
4	2427MHz	V	V	V	V
5	2432MHz	V	V	V	V
6	2437MHz	V	V	V	V
7	2442MHz	V	V	V	V
8	2447MHz	V	V	V	V
9	2452MHz	V	V	V	V
10	2457MHz	V	V	V	V
11	2462MHz	V	V	V	V
12	2467MHz			V	V
13	2472MHz			V	V
14	2484MHz				V

KEY: US = United States, CA = Canada, EU = European Countries (except France and Spain)

JP = Japan. Many countries and region are currently revising the channel assignment.

V = Supported

4.4.2 Bluetooth

Figure 8 – BT Channel Assignment

Channel	Frequency	RF Channel
Europe & USA	2400~2483.5 MHz	Freq.=2402+k MHz k=0~78
Japan	2400~2483.5 MHz	Freq.=2402+k MHz k=0~78

Most Europe area except Spain and France.

4.4.3 Security

- Complete Security Features- WEP64/128, WPA, WPA2, 802.1x and 802.11i
- Cisco CCx Compliant

4.5 Audio

Intense PC system support analog and digital inputs/outputs via standard 3.5'' audio jacks. For system audio specifications refer to **Table 5**.

4.5.1 Audio Codec General Description

Intense PC incorporates Realtek ALC888S-VC2 audio codec. ALC888S-VC2 is a high-performance 7.1+2 Channel High Definition Audio Codec with two independent S/PDIF outputs. It feature ten DAC channels that simultaneously support 7.1 sound playback, plus independent stereo sound output (multiple streaming) through the front panel stereo outputs, and integrate two stereo ADCs that can support a stereo microphone, and feature Acoustic Echo Cancellation (AEC), Beam Forming (BF), and Noise Suppression (NS) for voice applications.

The ALC888S-VC2 supports 16/20/24-bit S/DPIF input and output functions with sampling rate of up to 192 kHz, offering easy connection of PCs to high quality consumer electronic products such as digital decoders and Minidisk devices. In addition to the standard (primary) S/PDIF output function, the ALC888S features another independent (secondary) S/PDIF-OUT output and converters that transport digital audio output to a High Definition Media Interface (HDMI) transmitter (becoming more common in high-end PCs).

All analog IO are input and output capable, and headphone amplifiers are also integrated at each analog output. All analog IOs can be re-tasked according to user's definitions, or automatically switched.

The ALC888S-VC2 support host audio controller from the Intel ICH series chipset, and also from any other HDA compatible audio controller. With EAX/Direct Sound 3D/I3DL2/A3D compatibility, and excellent software utilities like environment sound emulation, multiple-band software equalizer and dynamic range control, optional Dolby® Digital Live, DTS® CONNECT™, and Dolby® Home Theater programs, the ALC888S provides an excellent home entertainment package and game experience for PC users.

The ALC888S-VC2 meets the current WLP3.10 (Windows Logo Program) and future WLP requirements that become effective from 01 June 2008 (See Enhanced Features section below). The ALC888S-VC2 also conforms to Intel's Audio Codec low power state white paper and is ECR compliant.

4.5.2 Audio Codec Features

- Meets premium audio requirements for Microsoft WLP 3.10
- High-performance DACs with 97dB SNR (A-Weighting), ADCs with 90dB SNR (A-Weighting)
- Ten DAC channels support 16/20/24-bit PCM format for 7.1 sound playback, plus 2 channels of independent stereo sound output (multiple streaming) through the front panel output
- Two stereo ADCs support 16/20/24-bit PCM format recording simultaneously
- All DACs supports 16/20/24-bit, 44.1k/48k/96k/192kHz sample rate
- All ADCs supports 16/20/24-btt, 44.1k/48k/96k/192kHz sample rate

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- Two independent S/PDIF-OUT converters support 16/20/24-bit, 4.1k/48k/88.2k/96k/192kHz sample rate. One converter for normal S/PDIF output, the other outputs an independent digital stream to the HDMI transmitter
- One S/PDIF-IN converter supports 44.1k/48k/96k/192k Hz sample rate
- Two jack detection pins each designed to detect up to 4 jacks
- Extra jack detection pin for CD input when it is used as an optional line level input, S/PDIF input and output
- Supports legacy analog mixer architecture
- Wide range (–80dB ~ +42dB) volume control with 1.5dB resolution of analog to analog mixer gain
- Software selectable boost gain (+10/+20/+30dB) for analog microphone input
- All analog jacks are stereo input and output re-tasking for analog plug & play
- Built-in headphone amplifiers for each re-tasking jack
- Support stereo digital microphone interface to improve voice quality
- Integrates high pass filter to cancel DC offset generated from digital microphone
- Support low voltage IO for HDA Link (1.5V~3.3V)
- Intel low power ECR compliant, supports power status control for each analog converter and pin widgets, supports jack detection and wake up event in D3 mode

Figure 9 – Audio Codec Functional Block Diagram
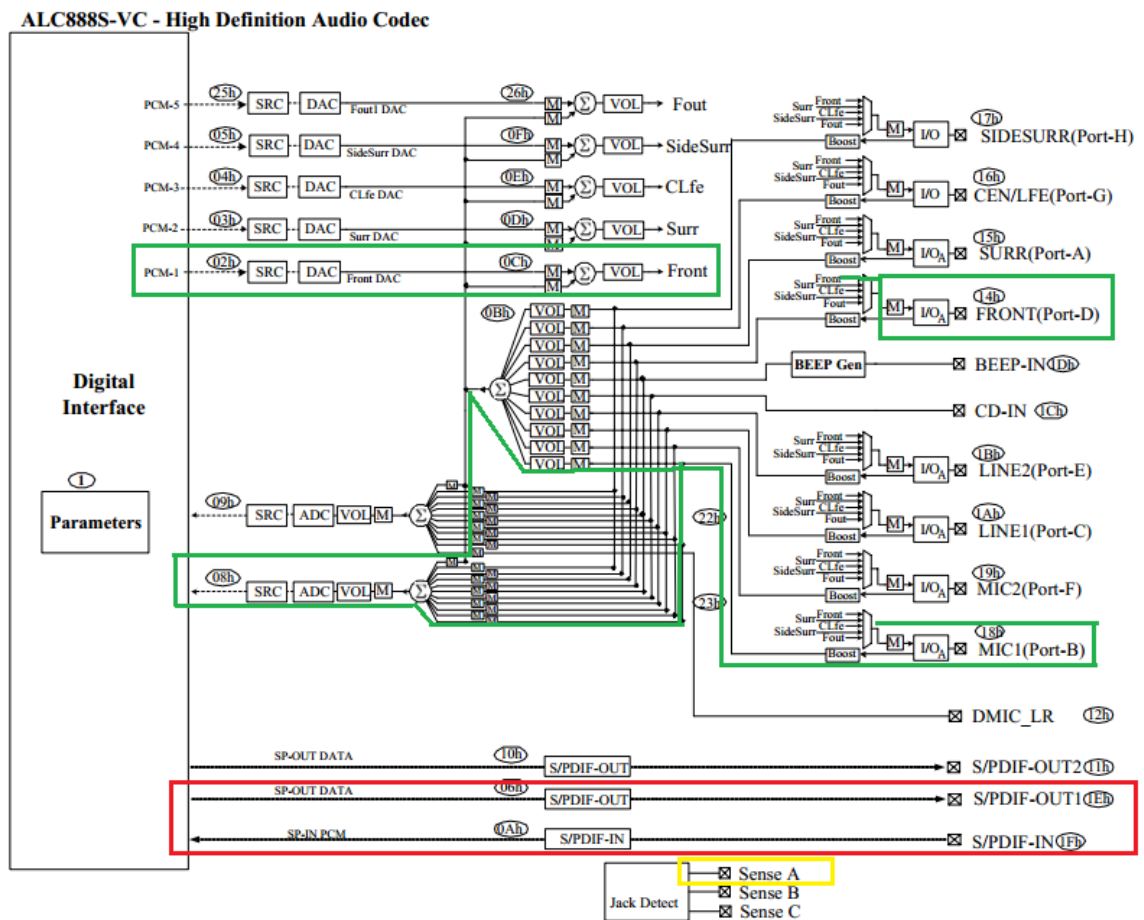
The markers in the **Figure 9** apply to audio functionality implemented in Intense PC system and summarized below:

1. Audio Jack Detect function implemented via Sense A:
2. Analog audio output: Port D, FRONT_HOUT_R/L (detect via 5k)
3. Analog audio input: Port B, MIC_IN_R/L (detected via 20k)
4. Digital audio output: S/PDIF-OUT1
5. Digital audio input: S/PDIF-IN

4.6 Super-I/O Controller

Intense PC design provides RS232 serial communication between Data Terminal Equipment (Host) and Data Communication Equipment (Device) by the means of Super-I/O Controller SMSC SIO1007, which implements LPC Bus to UART Bridge. The SIO1007 implements the LPC interface with the LPC PortSwitch interface. The LPC PortSwitch interface is a hot switchable external docking LPC interface. It also features a full 16bit internally decoded address bus, a Serial IRQ interface with PCI clock support, relocatable configuration ports and three DMA channel options.

The SIO1007 incorporates one complete 8-pin UART. In addition SIO1007 provides a second UART to support a serial Infrared interface that complies with IrDA v1.2 (Fast IR) and several other popular IR formats.

- **Main Features**
  - One full function Serial port
  - High Speed UART with Send/Receive 16-Byte FIFOs
  - Support 230k and 460k Baud rates
  - Programmable baud rate generator
  - Modem control circuit
  - IR communication controller
  - LPC bus Host interface
  - LPC PortSwitch interface
  - Two IRQ input pins
  - PC99a and ACPI 1.0 Compliant
  - Intelligent Auto Power Management
  - 16x GPIOs

Figure 10 – SMSC SIO1007 Super-I/O Controller functional block diagram

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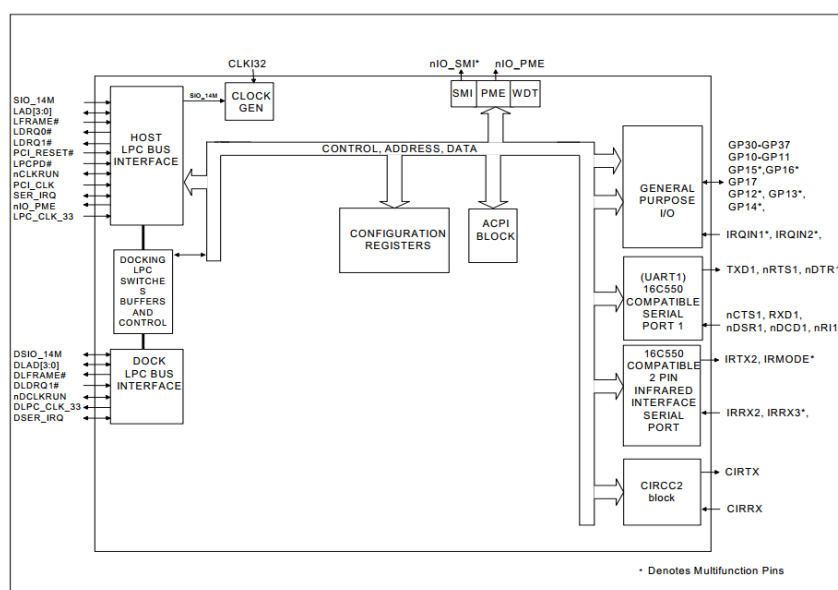
5 Interfaces

5.1 PCI Express*

This section describes the PCI Express interface capabilities of the processor. See the PCI Express Base Specification for details of PCI Express. The processor has one PCI Express controller that can support one external x8 PCI Express Graphics Device. The primary PCI Express Graphics port is referred to as PEG 0.

5.1.1 PCI Express* Architecture

Compatibility with the PCI addressing model is maintained to ensure that all existing applications and drivers may operate unchanged.

The PCI Express configuration uses standard mechanisms as defined in the PCI Plug-and-Play specification. The processor external graphics ports support Gen 3 speed as well. At 8 GT/s, Gen 3 operation results in twice as much bandwidth per lane as compared to Gen 2 operation. The 8-lane PCI Express* graphics port can operate at either 2.5 GT/s, 5 GT/s, or 8 GT/s.

PCI Express* Gen 3 uses a 128/130b encoding scheme, eliminating nearly all of the overhead of the 8b/10b encoding scheme used in Gen 1 and Gen 2 operation.

5.1.2 PCI Express* Specifications

- The port may negotiate down to narrower widths.
  Support for x8/x4/x2/x1 widths for a single PCI Express* mode.
- 2.5 GT/s, 5.0 GT/s and 8.0 GT/s PCI Express* frequencies are supported.
- Gen1 Raw bit-rate on the data pins of 2.5 GT/s, resulting in a real bandwidth per pair of 250 MB/s given the 8b/10b encoding used to transmit data across this interface. This also does not account for packet overhead and link maintenance.
- Maximum theoretical bandwidth on the interface of 4 GB/s in each direction simultaneously, for an aggregate of 8 GB/s when x8 Gen 1.
- Gen 2 Raw bit-rate on the data pins of 5.0 GT/s, resulting in a real bandwidth per pair of 500 MB/s given the 8b/10b encoding used to transmit data across this interface. This also does not account for packet overhead and link maintenance.
- Maximum theoretical bandwidth on the interface of 8 GB/s in each direction simultaneously, for an aggregate of 16 GB/s when x8 Gen 2.
- PCI Express* reference clock is 100-MHz differential clock.
- Power Management Event (PME) functions.
- Dynamic width capability.
- Polarity inversion.
- Supports Half Swing "low-power/low-voltage".

Note: The Ivy Bridge processor does not support PCI Express* Hot-Plug.

5.1.3 Mini PCI Express* Edge Connector

Table 20 – mini PCI Express edge connector pinout

		mini PCI Express edge connector			
Pin #	Pin Name	Signal Description	Pin #	Pin Name	Signal Description
1	WAKE#	Open drain, active low signal driven low by a mini PCIe card to reactivate the PCIe link	2	3.3Vaux	3.3V power rail
3	COEX1/Reserved	Reserved for future wireless coexistence control interface between radios (if needed)	4	GND	Ground connection
5	COEX2/Reserved		6	1.5V	1.5V power rail
7	CLKREQ#	Clock request - open drain, active low driven by mini PCIe card to request PCIe reference clock	8	UIM_PWR/Reserved	
9	GND	Ground connection	10	UIM_DATA/Reserved	
11	REFCLK-	PCI Express differential reference clock (100 MHz)	12	UIM_CLK/Reserved	The UIM signals are defined on the system connector to provide the interface between the removable User Identity Module (UIM) Interface - an extension of SIM and WWAN.
13	REFCLK+		14	UIM_RESET/Reserved	
15	GND	Ground connection	16	UIM_VPP/Reserved	
		Mechanical Notch Key			
17	Reserved/UIM_C8	Reserved	18	GND	Ground connection
19	Reserved/UIM_C4	Reserved	20	W_DISABLE#	Active low signal when asserted by the system disable radio operation. Reserved for future use.
21	GND	Ground connection	22	PERST#	Asserted when power is switched off and also can be used by the system to force HW reset
23	PERn0		24	3.3Vaux	3.3V power rail
25	PERp0	PCI Express differential receive pair	26	GND	Ground connection
27	GND	Ground connection	28	1.5V	1.5V power rail
29	GND	Ground connection	30	SMB_CLK	Optional SMBus two-wire interface for Host/mini PCIe module communication
31	PETn0		32	SMB_DATA	
33	PETp0	PCI Express differential transmit pair	34	GND	Ground connection
35	GND	Ground connection	36	USB_D-	
37	GND	Ground connection	38	USB_D+	USB Host Interface
39	3.3Vaux	3.3V power rail	40	GND	Ground connection
41	3.3Vaux	3.3V power rail	42	LED_WWAN#	
43	GND	Ground connection	44	LED_WLAN#	Active low output signals are provided to allow status indications to users via system provided LEDs
45	Reserved		46	LED_WPAN#	
47	Reserved		48	1.5V	1.5V power rail
49	Reserved		50	GND	Ground connection
51	Reserved	Reserved for future second PCI Express Lane	52	3.3Vaux	3.3V power rail

5.2 Direct Media Interface (DMI)

Direct Media Interface (DMI) connects the processor and the PCH. Next generation DMI 2.0 is supported.

5.2.1 DMI Specifications

- DMI 2.0 support
- Four lanes in each direction
- GT/s point-to-point DMI interface to PCH is supported
- Raw bit-rate on the data pins of 5.0 Gbps, resulting in a real bandwidth per pair of 500 MB/s given the 8b/10b encoding used to transmit data across this interface. Does not account for packet overhead and link maintenance.
- Maximum theoretical bandwidth on interface of 2 GB/s in each direction simultaneously, for an aggregate of 4 GB/s when DMI x4
- Shares 100-MHz PCI Express* reference clock
- DC coupling – no capacitors between the processor and the PCH
- Polarity inversion
- PCH end-to-end lane reversal across the link
- Supports Half Swing "low-power/low-voltage"

5.3 Flexible Display Interface (FDI)

The Intel Flexible Display Interface (Intel FDI) is a proprietary link for carrying display traffic from the Processor Graphics controller to the PCH display I/O. Intel FDI supports two or three independent channels – one for pipe A, one for pipe B and one for Pipe C.

Channels A and B has maximum of four transmit (Tx) differential pairs used for transporting pixel and framing data from the display engine in two display configuration. In three display configuration Channel A has 4 transmit (Tx) differential pairs while Channel B and C has two transmit (Tx) differential pairs.

5.3.1 FDI Specifications

- For SKUs with graphics, carries display traffic from the Processor Graphics in the processor to the legacy display connectors in the PCH
- Based on DisplayPort standard
- The two FDI links are capable of being configured to support three independent channels, one for each display pipeline
- There are two FDI channels, each one consists of four unidirectional downstream differential transmitter pairs:
  — Scalable down to 3x, 2x, or 1x based on actual display bandwidth requirements
  — Fixed frequency 2.7 GT/s data rate
- Two sideband signals for Display synchronization:
  — FDI_FSYNC and FDI_LSYNC (Frame and Line Synchronization)
- One Interrupt signal used for various interrupts from the PCH:
  — FDI_INT signal shared by both Intel FDI Links

- PCH supports end-to-end lane reversal across both links
- Common 100-MHz reference clock
- Each channel transports at a rate of 2.7 Gbps
- PCH supports end-to-end lane reversal across both channels (no reversal support required in the processor)

5.4 Digital Display Interface

The PCH can drive a number of digital interfaces natively. The Digital Ports B, C, and/or D can be configured to drive HDMI, DVI, DisplayPort, and Embedded DisplayPort (port D only). The PCH provides a dedicated port for Digital Port LVDS.

Intense PC LVDS display interface routed to FACE Modules connectors.

5.4.1 LVDS Display Interface

LVDS for flat panel is compatible with the ANSI/TIA/EIA-644 specification. This is an electrical standard only defining driver output characteristics and receiver input characteristics.

Each channel supports transmit clock frequency ranges from 25 MHz to 112 MHz, which provides a throughput of up to 784 Mbps on each data output and up to 112 MP/s on the input. When using both channels, each carry a portion of the data; thus, doubling the throughput to a maximum theoretical pixel rate of 224 MP/s.

The LVDS data pair is used to transfer pixel data as well as the LCD timing control signals.

5.4.2 High Definition Multimedia Interface (HDMI)

The High-Definition Multimedia Interface (HDMI) is provided for transmitting uncompressed digital audio and video signals from DVD players, set-top boxes and other audiovisual sources to television sets, projectors and other video displays. It can carry high quality multi-channel audio data and all standard and high-definition consumer electronics video formats. HDMI display interface connecting the PCH and display devices utilizes transition minimized differential signaling (TMDS) to carry audiovisual information through the same HDMI cable.

HDMI includes three separate communications channels: TMDS, DDC, and the optional CEC (consumer electronics control) which is not supported by the PCH. As shown in **Figure 11** the HDMI cable carries four differential pairs that make up the TMDS data and clock channels. These channels are used to carry video, audio, and auxiliary data. In addition, HDMI carries a VESA DDC. The DDC is used by an HDMI Source to determine the capabilities and characteristics of the Sink.

Audio, video and auxiliary (control/status) data is transmitted across the three TMDS data channels. The video pixel clock is transmitted on the TMDS clock channel and is used by the receiver for data recovery on the three data channels. The digital display data signals driven natively through the PCH are AC coupled and needs level shifting to convert the AC coupled signals to the HDMI compliant digital signals. PCH HDMI interface is designed as per High-Definition Multimedia Interface Specification 1.4a.

Figure 11 – HDMI Link Diagram
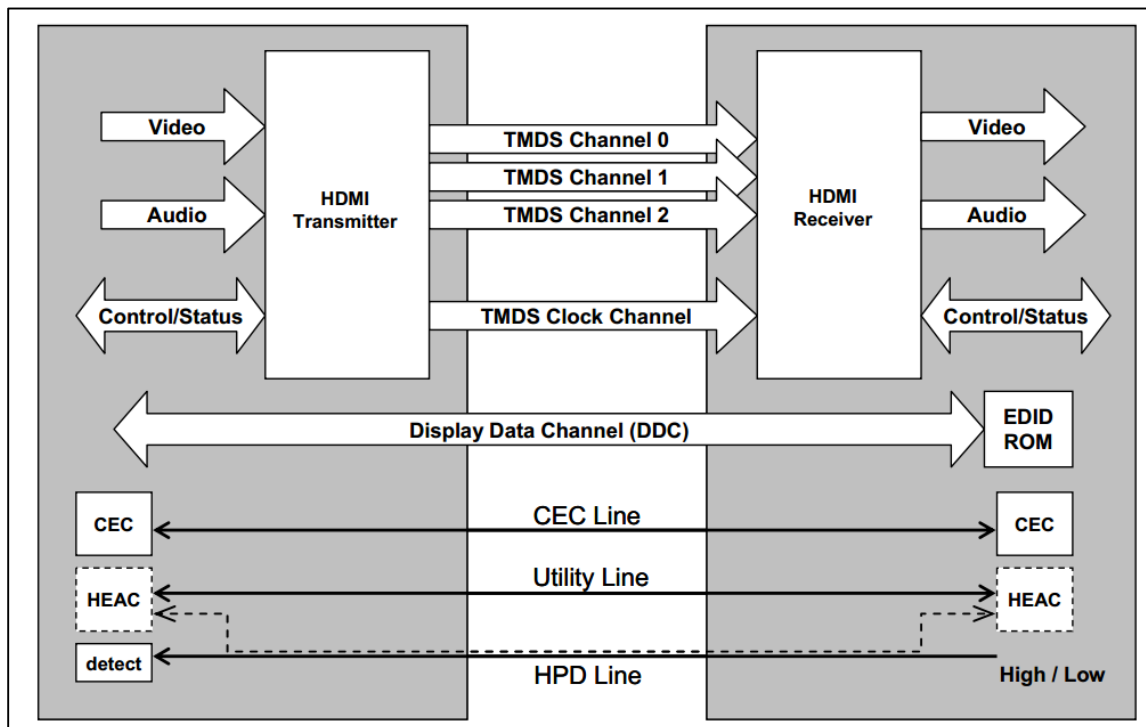
5.4.2.1 HDMI Connector

Table 21 shows the pin assignments of the HDMI external connector on a Downstream port on a Source device (Intense PC).

Table 21 – Downstream Port HDMI Connector Pinout

Pin #	Signal	Pin #	Signal
1	TMDS_DATA2+	2	TMDS_DATA2 Shield
3	TMDS_DATA2-	4	TMDS_DATA1+
5	TMDS_DATA1 Shield	6	TMDS_DATA1-
7	TMDS_DATA0+	8	TMDS_DATA0 Shield
9	TMDS_DATA0-	10	TMDS_CLK+
11	TMDS_CLK Shield	12	TMDS_CLK-
13	CEC	14	Reserved
15	DDC_SCL	16	DDC_SDA
17	GND	18	PWR_5V
19	HPD		

Table 22 – Downstream Port HDMI Connector Signal Description

Pin #	Signal	Source Direction	Description
1	TMDS_DATA2+	Out	
2	TMDS_DATA2 Shield	-	
3	TMDS_DATA2-	Out	Data differential pair 2 - Link 1
4	TMDS_DATA1+	Out	
5	TMDS_DATA1 Shield	-	
6	TMDS_DATA1-	Out	Data differential pair 1 - Link 1
7	TMDS_DATA0+	Out	
8	TMDS_DATA0 Shield	-	
9	TMDS_DATA0-	Out	Data differential pair 0 - Link 1
10	TMDS_CLK+	Out	
11	TMDS_CLK Shield	-	
12	TMDS_CLK-	Out	Clock differential pair - Link 1
13	CEC	In/Out	Consumer Electronics Control
14	Reserved	-	
15	DDC_SCL	Out	
16	DDC_SDA	In/Out	EDID Communication channel
17	GND	-	Ground
18	PWR_5V	Out	Power
19	HPD	In	Hot Plug Detect

5.4.3 Digital Video Interface (DVI)

The PCH Digital Ports can be configured to drive DVI-D. DVI uses TMDS for transmitting data from the transmitter to the receiver which is similar to the HDMI protocol but without the audio and CEC. Refer to the HDMI section for more information on the signals and data transmission. To drive DVI-I through the back panel the VGA DDC signals is connected along with the digital data and clock signals from one of the Digital Ports. The digital display data signals driven natively through the PCH are AC coupled and needs level shifting to convert the AC coupled signals to the HDMI compliant digital signals.

5.4.4 Display Port Interface (DP)

DisplayPort is a digital communication interface that utilizes differential signaling to achieve a high bandwidth bus interface designed to support connections between PCs and monitors, projectors, and TV displays. DisplayPort is also suitable for display connections between consumer electronics devices such as high definition optical disc players, set top boxes, and TV displays.

A DisplayPort consists of a Main Link, Auxiliary channel, and a Hot Plug Detect signal. The Main Link is a unidirectional, high-bandwidth, and low latency channel used for transport of

isochronous data streams such as uncompressed video and audio. The Auxiliary Channel (AUX CH) is a half-duplex bidirectional channel used for link management and device control. The Hot Plug Detect (HPD) signal serves as an interrupt request for the sink device.

PCH is designed as per VESA DisplayPort Standard Version 1.1a.

Figure 12 – DP Link Diagram
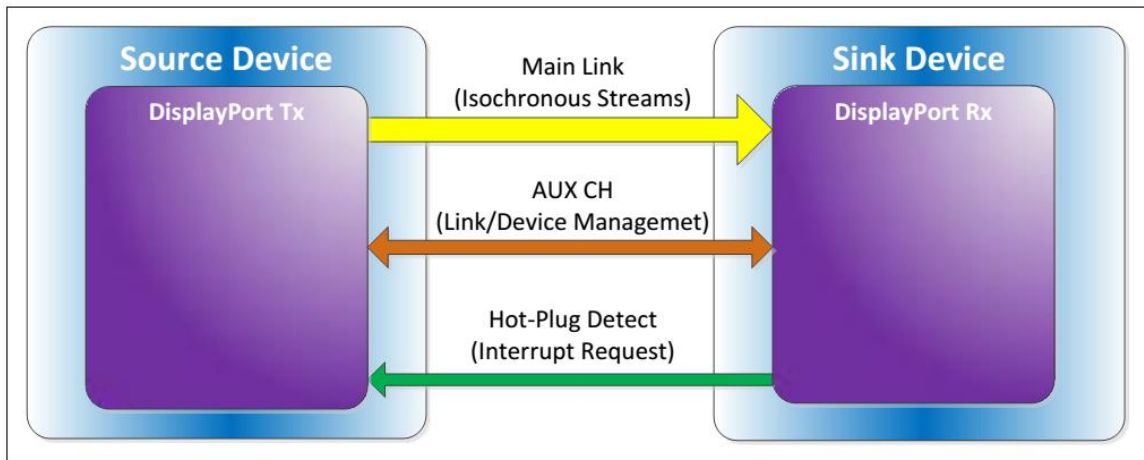
5.4.4.1 DisplayPort Connector

Table 23 shows the pin assignments of the DisplayPort external connector on a downstream port on a Source device (Intense PC) and Table 24 show the pin assignments of the DisplayPort external connector on an upstream port on a Sink device (DisplayPort Monitor).

Table 23 – Downstream Port DP Connector Pinout

Pin Number	Signal Type	Pin Name	Mating Row Contact Location	Vertically Opposed Connector's Front View
1	Out	ML_Lane 0(p)	Top	
2	GND	GND	Bottom	
3	Out	ML_Lane 0 (n)	Top	
4	Out	ML_Lane 1 (p)	Bottom	
5	GND	GND	Top	
6	Out	ML_Lane 1 (n)	Bottom	
7	Out	ML_Lane 2 (p)	Top	
8	GND	GND	Bottom	
9	Out	ML_Lane 2 (n)	Top	
10	Out	ML_Lane 3 (p)	Bottom	
11	GND	GND	Top	
12	Out	ML_Lane 3 (n)	Bottom	
13	CONFIG (see note 1)	CONFIG1	Top	
14	CONFIG (see note 1)	CONFIG2	Bottom	
15	I/O	AUX CH (p)	Top	
16	GND	GND	Bottom	
17	I/O	AUX CH (n)	Top	
18	In	Hot Plug Detect	Bottom	
19	RTN	Return	Top	
20	PWR Out (see note 2)	DP_PWR	Bottom	

Notes:

1. Pins 13 and 14 must be connected to ground through a pull-down device. External devices and cable assemblies must be designed to not rely on a low impedance ground path from these pins.
2. Pin 20, PWR Out, must provide +3.3V+/-10% with a maximum current of 500mA and a minimum power capability of 1.5 watts.

Table 24 – Upstream Port DP Connector Pinout

Pin Number	Signal Type	Pin Name	Mating Row Contact Location	Vertically Opposed Connector's Front View
1	In	ML_Lane 3(n)	Top	
2	GND	GND	Bottom	
3	In	ML_Lane 3 (p)	Top	
4	In	ML_Lane 2 (n)	Bottom	
5	GND	GND	Top	
6	In	ML_Lane 2 (p)	Bottom	
7	In	ML_Lane 1 (n)	Top	
8	GND	GND	Bottom	
9	In	ML_Lane 1 (p)	Top	
10	In	ML_Lane 0 (n)	Bottom	
11	GND	GND	Top	
12	In	ML_Lane 0 (p)	Bottom	
13	CONFIG (see note 1)	CONFIG1	Top	
14	CONFIG (see note 1)	CONFIG2	Bottom	
15	I/O	AUX CH (p)	Top	
16	GND	GND	Bottom	
17	I/O	AUX CH (n)	Top	
18	Out	Hot Plug Detect	Bottom	
19	RTN	Return	Top	
20	Power Out (see note 2)	DP_PWR	Bottom	

Notes:

1. Pins 13 and 14 must be connected to ground through a pull-down device. External devices and cable assemblies must be designed to not rely on a low impedance ground path from these pins.
2. Pin 20, PWR Out, must provide +3.3 volts ±10% with a maximum current of 500mA and a minimum power capability of 1.5 watts.

Table 25 shows the wiring of an external cable connector assembly.

Table 25 – Display Port Cable

Receptacle On Source Device (At SOURCE – Signal Type)	Pin#	Source Side Plug (At SOURCE – Signal Type)	Pin#	Sink Side Plug – Pin#	Sink Side Plug (At SINK – Signal Type)	Receptacle on the Sink Device – Pin#	Sink End Dongle (Signal Type)
Out – ML_Lane 0(p)	1	Out – ML_Lane 0(p)	1	1	ML_Lane 3 (n) – In	1	ML_Lane 3 (n) – In
GND – GND	2	GND – GND	2	2	GND – GND	2	GND – GND
Out – ML_Lane 0 (n)	3	Out – ML_Lane 0 (n)	3	3	ML_Lane 3 (p) – In	3	ML_Lane 3 (p) – In
Out – ML_Lane 1 (p)	4	Out – ML_Lane 1 (p)	4	4	ML_Lane 2 (n) – In	4	ML_Lane 2 (n) – In
GND – GND	5	GND – GND	5	5	GND – GND	5	GND – GND
Out – ML_Lane 1 (n)	6	Out – ML_Lane 1 (n)	6	6	ML_Lane 2 (p) – In	6	ML_Lane 2 (p) – In
Out – ML_Lane 2 (p)	7	Out – ML_Lane 2 (p)	7	7	ML_Lane 1 (n) – In	7	ML_Lane 1 (n) – In
GND – GND	8	GND – GND	8	8	GND – GND	8	GND – GND
Out – ML_Lane 2 (n)	9	Out – ML_Lane 2 (n)	9	9	ML_Lane 1 (p) – In	9	ML_Lane 1 (p) – In
Out – ML_Lane 3 (p)	10	Out – ML_Lane 3 (p)	10	10	ML_Lane 0 (n) – In	10	ML_Lane 0 (n) – In
GND – GND	11	GND – GND	11	11	GND – GND	11	GND – GND
Out – ML_Lane 3 (n)	12	Out – ML_Lane 3 (n)	12	12	ML_Lane 0 (p) – In	12	ML_Lane 0 (p) – In
CONFIG – CONFIG1	13	CONFIG – CONFIG1	13	13	CONFIG1 – CONFIG	13	CONFIG1 – CONFIG
CONFIG – CONFIG2	14	CONFIG – CONFIG2	14	14	CONFIG2 – CONFIG	14	CONFIG2 – CONFIG
I/O – AUX_CH (p)	15	I/O – AUX_CH (p)	15	15	AUX_CH (p) – I/O	15	AUX_CH (p) – I/O
GND – GND	16	GND – GND	16	16	GND – GND	16	GND – GND
I/O – AUX_CH (n)	17	I/O – AUX_CH (n)	17	17	AUX_CH (n) – I/O	17	AUX_CH (n) – I/O
In – Hot Plug Detect	18	In – Hot Plug Detect	18	18	Hot Plug Detect – Out	18	Hot Plug Detect – Out
PWR RTN – Return DP_PWR	19	Return DP_PWR	19	19	Return DP_PWR	19	Return DP_PWR – PWR RTN
PWR Out – DP_PWR	20	DP_PWR	20	20	DP_PWR	20	DP_PWR – PWR Out

5.5 Analog Display Interface

The Analog Port provides RGB signal output along with a HSYNC and VSYNC signal. There is an associated Display Data Channel (DDC) signal pair that is implemented using GPIO pins dedicated to the Analog Port. The intended target device is for a monitor with a VGA connector. Display devices such as LCD panels with analog inputs may work satisfactory but no functionality added to the signals to enhance that capability.

5.5.1 VGA FPC Connector

For an analog interface Intense PC uses 0.5mm pitch Right angle FPC connector with 20 downside contacts. Manufacturer and P/N: CVILux CF20-201D0R0.

Table 26 – VGA FPC Connector

Pin #	Signal	Source Direction	Description
1	5V	Out	Power
2	DDC_SDA	In/Out	EDID Communication channel
3	DDC_SCL	Out	
4	3.3V	Out	Power
5	GND	-	
6	SIO_GPIO17	In/Out	General Purpose SuperIO Controller I/Os
7	SIO_GPIO32	In/Out	
8	SIO_GPIO33	In/Out	
9	SIO_GPIO34	In/Out	
10	GND	-	Ground
11	VGA_HSYNC	Out	Horizontal sync signal
12	GND	-	Ground
13	VGA_VSYNC	Out	Vertical sync signal
14	GND	-	Ground
15	VGA_BLUE	Out	Analog blue information
16	GND	-	Ground
17	VGA_GREEN	Out	Analog green information
18	GND	-	Ground
19	VGA_RED	Out	Analog red information
20	GND	-	Ground

Note: VGA FPC connector is not assembled by default but available for custom orders with MOQ (minimum order quantity) > 100 units.

5.6   RS232 Serial Interface

Intense PC design provides RS232 serial communication port (COM1) and support six RS232 signal set by the means of Super-I/O Controller described in 4.6 and RS232/UART line driver transceiver device. Due to small dimension physical port is implemented with ultra mini serial connector with the pinout in the table below.

Table 27 – COM1 Serial Port Pinout

Pin #	Signal	Host Direction	Description
1	COM1_TX	Out	Transmit Data – Carries data from DTE to DCE
2	COM1_RTS	Out	Request To Send – DTE requests the DCE prepare to receive data
3	COM1_RX	In	Receive Data – Carries data from DCE to DTE
4	COM1_CTS	In	Clear To Send – Indicates DCE is ready to accept data
5	COM1_DTR	Out	Data Terminal Ready – Indicates presence of DTE to DCE
6	COM1_DSR	In	Data Set Ready – DCE is ready to receive commands or data
7	COM1_RI	N/A	Ring Indicator is not supported
8	GND	-	Ground

6 Miscellaneous Features

6.1 Mini PCI Express/mSATA sharing

Intense PC advanced platform components and Compulab's flexible system design offers extremely high utilization of different functionalities and mechanical Form Factors to be implemented on the same HW.

Mini PCIe and mSATA share the same slot, and allow the flexibility to install both storage and PCI express devices. PCI Express/SATA interface switching implemented with 4-channel differential bi-directional multiplexer/de-multiplexer as shown in **Figure 13**.

Note: Proper functionality requires BIOS configuration to set the MUX to desired connectivity option (in default mSATA).

Figure 13 – Intense PC Mini PCIe/mSATA scheme
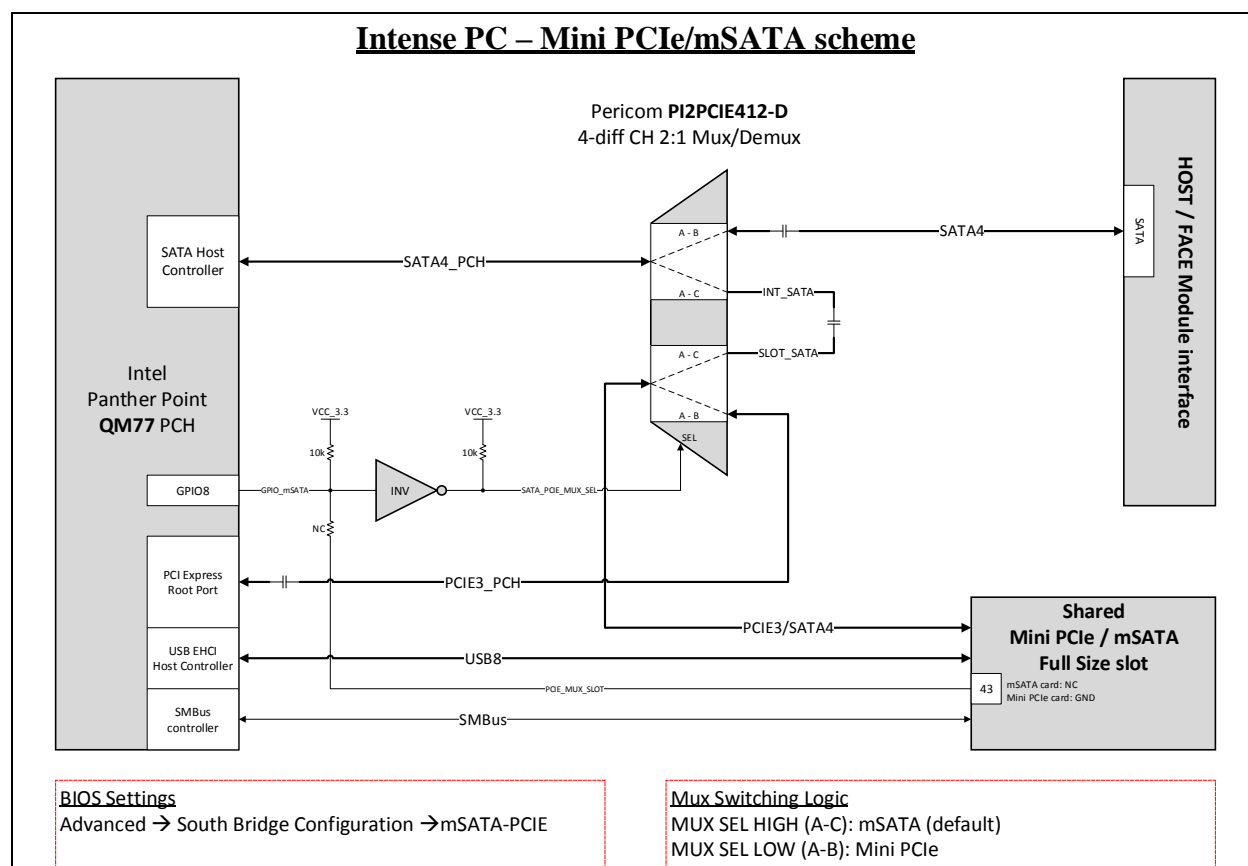
6.2 SPI Interface

The main functionality of SPI bus is initialization, configuration of HW components and BIOS execution during system power up.

Two Serial NOR flash (SNOR) devices stores system CONFIG and BIOS code.

Attention: Intense PC SPI interface used for system configuration purposes only and restricted for customer use. Data provided in this section is informative only. Any violation of the design, by the use of other SPI slave devices may result in system failures and void of warranty.

6.3 FACE Module Interface

FACE Module (**F**unction **A**nd **C**onnectivity **E**xtension Module) designed as additional/optional system board providing extended functionality and IO connectivity options. The interface between main system board and FACE module implemented with high speed, low pitch, and high pin count board-to-board connectors (B2B). Connectors' pinout including signals mapping and description described later in this chapter.

Figure 14 – FACE Module concept
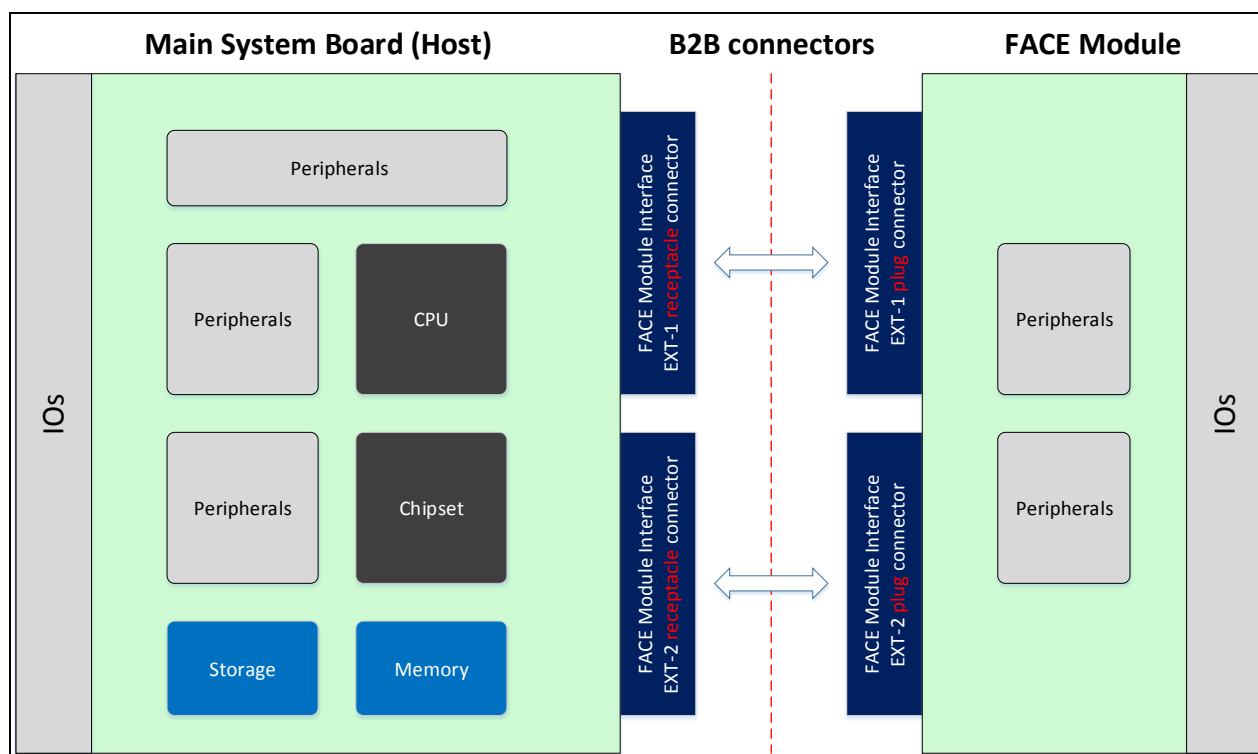
6.3.1 Extension Connectors

Complete B2B receptacle and plug connector's specifications shown in the tables below.

Table 28 – B2B receptacle connector HOST side

Item	Option A	Option B	Option C
Manufacturer	FCI	Tyco	Oupiin
PN	61082-10260	5-5179180-4	2382-100C00DP1T-M
Type	Receptacle	Receptacle	Receptacle
Positions	2x50	2x50	2x50
Pitch	0.8mm	0.8mm	0.8mm
Current rating	0.5A	0.5A	0.5A
Height	7.7mm	7.7mm	7.7mm
Stacking height	12mm	12mm	12mm

Table 29 – B2B plug connector FACE Module side

Item	Option A	Option B	Option C
Manufacturer	FCI	Tyco	Oupiin
PN	61083-10460	3-5177986-4	2381-100C00DP4T-M
Type	Plug	Plug	Plug
Positions	2x50	2x50	2x50
Pitch	0.8mm	0.8mm	0.8mm
Current rating	0.5A	0.5A	0.5A
Height	7.7mm	7.7mm	7.7mm
Stacking height	12mm	12mm	12mm

6.3.2 Connectors Pinout

The tables below provide complete pinout of extension connectors EXT1, EXT2 and signals mapping.

Table 30 – EXT1 connector HOST side pinout

		EXT-1 connector HOST side				
Pin #	**Pin Name**	**Signal Description**	**Pin #**	**Pin Name**	**Signal Description**	
A1	GND	Ground connection	B1	GND	Ground connection	
A2	SATA2_TX+	SATA2.0 differential transmit pair 2; Host signal shared with mini PCIe (MUX channel B)	B2	SATA0_TX+/CLK+	Host PEG CLK output differential pair - 100MHz PCIe Gen2 to PCIe Graphics device[1]	
A3	SATA2_TX-		B3	SATA0_TX-/CLK-		
A4	IR_RX	IR UART receive signal	B4	SATA0_LED	SATA activity LED indicator	
A5	SATA2_RX+	SATA2.0 differential receive pair 2; Host signal shared with mini PCIe (MUX channel B)	B5	SATA0_RX+/CLK+	Host PCIe CLK output differential pair - 100MHz PCIe Gen2 to PCIe devices	
A6	SATA2_RX-		B6	SATA0_RX-/CLK-		
A7	GND	Ground connection	B7	V5SBY	5V power domain	
A8	SATA3_TX+	SATA2.0 differential transmit pair 3	B8	SATA1_RX+	SATA3.0 differential receive pair 1	
A9	SATA3_TX-		B9	SATA1_RX-		
A10	SMB_ALRT#	SMBus Alert used to wake the system	B10	DEBUG1	Reserved debug signal	
A11	SATA3_RX+	SATA2.0 differential receive pair 3	B11	SATA1_TX+	SATA3.0 differential transmit pair 1	
A12	SATA3_RX-		B12	SATA1_TX-		
A13	V5SBY	5V power domain	B13	V5SBY	5V power domain	
A14	SMB_CLK	SMBus host clock output. Connect to SMBus slave.	B14	USB3_P	USB Host interface 3	
A15	SMB_DAT	SMBus bidirectional data. Connect to SMBus slave.	B15	USB3_N		
A16	HDA_RST#	High Definition Audio host reset	B16	USB_OC_2_3#	USB Overcurrent Indicator for lanes 2/3	
A17	HDA_SYNC	High Definition Audio host sync	B17	USB2_P	USB Host interface 2	
A18	HDA_BITCLK	High Definition Audio host bit clock out 24MHz	B18	USB2_N		
A19	HDA_SDOUT	High Definition Audio serial host data out	B19	V5SBY	5V power domain	
A20	HDA_SDIN1	High Definition Audio serial host data in1	B20	Reserved	Reserved for internal test purposes	
A21	HDA_SDIN0	High Definition Audio serial host data in0	B21	Reserved	Reserved for internal test purposes	
A22	DEBUG3	Reserved debug signal	B22	LPC_SERIRQ	Serial Interrupt Request	
A23	GND	Ground connection	B23	LPC_CLK	Single Ended 33MHz CLK host out to PCI devices	
A24	USB0_P	USB Host interface lane 0	B24	LPC_FRAME#	LPC interface frame signal	
A25	USB0_N		B25	GND	Ground connection	
A26	USB_OC0_1#	USB Overcurrent Indicator for lanes 0/1	B26	Reserved	Reserved for internal use only	
A27	USB1_P	USB Host interface 1	B27	Reserved	Reserved for internal use only	
A28	USB1_N		B28	Reserved	Reserved for internal use only	
A29	GND	Ground connection	B29	Reserved	Reserved for internal use only	
A30	LPC_AD0	LPC bus multiplexed command, address and data. Internal PU provided on LPC[3:0]	B30	Reserved	Reserved for internal use only	
A31	LPC_AD1		B31	RESET#	Active Low Platform Reset driven by the Host	
A32	LPC_AD2		B32	PCIE_CLK+	Host PCIe CLK output differential pair - 100MHz PCIe Gen2 to PCIe devices	
A33	LPC_AD3		B33	PCIE_CLK-		

A34	GND	Ground connection	B34	EXT_PRSNT#	Clock Request for PCI Express 100 MHz Clocks
A35	PCIE_TX3+	PCI Express (x1) Gen2 (up to 5Gbps) differential transmit pair 3	B35	PCIE_RX3+	PCI Express (x1) Gen2 (up to 5Gbps) differential receive pair 3
A36	PCIE_TX3-		B36	PCIE_RX3-	
A37	PCIE_WAKE#	PCI Express Wake Event from Device to Host	B37	SPI_EXT_CNTRL	SPI interface external control signal
A38	PCIE_TX2+	PCI Express (x1) Gen2 (up to 5Gbps) differential transmit pair 2	B38	PCIE_RX2+	PCI Express (x1) Gen2 (up to 5Gbps) differential receive pair 2
A39	PCIE_TX2-		B39	PCIE_RX2-	
A40	GND	Ground connection	B40	GND	Ground connection
A41	PCIE_TX1+	PCI Express (x1) Gen2 (up to 5Gbps) differential transmit pair 1	B41	PCIE_RX1+	PCI Express (x1) Gen2 (up to 5Gbps) differential receive pair 1
A42	PCIE_TX1-		B42	PCIE_RX1-	
A43	PWRBTN#	System power button signal	B43	SLP#	Assert LP state S3 (sleep) active low signal
A44	PCIE_TX0+	Host CPU PEG (x1) - PCIe Gen3 (up to 8Gbps) differential transmit pair for external graphics	B44	PCIE_RX0+	Host CPU PEG (x1) - PCIe Gen3 (up to 8Gbps) differential receive pair for external graphics
A45	PCIE_TX0-		B45	PCIE_RX0-	
A46	RESERVED	Reserved debug signal	B46	RESERVED	Reserved debug signal
A47	VCC_12V		B47	VCC_12V	
A48	VCC_12V		B48	VCC_12V	
A49	VCC_12V		B49	VCC_12V	
A50	VCC_12V	Main 12V power domain	B50	VCC_12V	Main 12V power domain

Table 31 – EXT2 connector HOST side pinout

EXT-2 connector HOST side					
Pin #	Pin Name	Signal Description	Pin #	Pin Name	Signal Description
A1	GND	Ground connection	B1	GND	Ground connection
A2	PEG_RX0+/RSVD0	Host CPU PEG_0 (x8) - PCIe Gen3 (up to 8Gbps) differential receive pair for external graphics	B2	PEG_TX0+/RSVD6	Host CPU PEG_0 (x8) - PCIe Gen3 (up to 8Gbps) differential transmit pair for external graphics
A3	PEG_RX0-/RSVD1		B3	PEG_TX0-/RSVD7	
A4	DGPU_PRSNT#/RSVD3	Host chipset GPIO67, Input, PU-10k	B4	DGPU_PWREN#/RSVD8	Host chipset GPIO54, Output, PU-8.2k
A5	PEG_RX1+/RSVD4	Host CPU PEG_1 (x8) - PCIe Gen3 (up to 8Gbps) differential receive pair for external graphics	B5	PEG_TX1+/RSVD9	Host CPU PEG_1 (x8) - PCIe Gen3 (up to 8Gbps) differential transmit pair for external graphics
A6	PEG_RX1-/RSVD5		B6	PEG_TX1-/RSVD10	
A7	GND	Ground connection	B7	GND	Ground connection
A8	PEG_RX2+/RSVD11	Host CPU PEG_2 (x8) - PCIe Gen3 (up to 8Gbps) differential receive pair for external graphics	B8	PEG_TX2+/RSVD16	Host CPU PEG_2 (x8) - PCIe Gen3 (up to 8Gbps) differential transmit pair for external graphics
A9	PEG_RX2-/RSVD12		B9	PEG_TX2-/RSVD17	
A10	DGPU_PWROK/RSVD13	Host chipset GPIO17, Input/Output, PD-10k	B10	DGPU_HOLD_RST#/RSVD18	Host chipset GPIO50, Output, PU-8.2k
A11	PEG_RX3+/RSVD14	Host CPU PEG_3 (x8) - PCIe Gen3 (up to 8Gbps) differential receive pair for external graphics	B11	PEG_TX3+/RSVD19	Host CPU PEG_3 (x8) - PCIe Gen3 (up to 8Gbps) differential transmit pair for external graphics
A12	PEG_RX3-/RSVD15		B12	PEG_TX3-/RSVD20	
A13	GND	Ground connection	B13	GND	Ground connection
A14	PEG_RX4+/RSVD21	Host CPU PEG_4 (x8) - PCIe Gen3 (up to 8Gbps) differential receive pair for external graphics	B14	PEG_TX4+/RSVD26	Host CPU PEG_4 (x8) - PCIe Gen3 (up to 8Gbps) differential transmit pair for external graphics
A15	PEG_RX4-/RSVD22		B15	PEG_TX4-/RSVD27	

A16	DGPU_SELECT#/RSVD23	Host chipset GPIO52, Output, PU-8.2k		B16	DGPU_HPD_INTR#/RSVD28	Host chipset GPIO6, Input, PU-10k
A17	PEG_RX5+/RSVD24	Host CPU PEG_5 (x8) - PCIe Gen3 (up to 8Gbps) differential receive pair for external graphics		B17	PEG_TX5+/RSVD29	Host CPU PEG_5 (x8) - PCIe Gen3 (up to 8Gbps) differential transmit pair for external graphics
A18	PEG_RX5-/RSVD25			B18	PEG_TX5-/RSVD30	
A19	V5SBY	5V power domain		B19	V5SBY	5V power domain
A20	PEG_RX6+/RSVD31	Host CPU PEG_6 (x8) - PCIe Gen3 (up to 8Gbps) differential receive pair for external graphics		B20	PEG_TX6+/RSVD36	Host CPU PEG_6 (x8) - PCIe Gen3 (up to 8Gbps) differential transmit pair for external graphics
A21	PEG_RX6-/RSVD32			B21	PEG_TX6-/RSVD37	
A22	DGPU_PWM_SELECT#/RSVD33	Host chipset GPIO53, Output, No pull		B22	SPARE/eDP_HDP	NC
A23	PEG_RX7+/RSVD34	Host CPU PEG_7 (x8) - PCIe Gen3 (up to 8Gbps) differential receive pair for external graphics		B23	PEG_TX7+/RSVD38	Host CPU PEG_7 (x8) - PCIe Gen3 (up to 8Gbps) differential transmit pair for external graphics [2]
A24	PEG_RX7-/RSVD35			B24	PEG_TX7-/RSVD39	
A25	GND	Ground connection		B25	GND	Ground connection
A26	LVDS_A0+/eDP_TX0+	LVDS Channel A differential pair 0 Host data output		B26	PEG_CLK+/RSVD40	Host PEG CLK output differential pair - 100MHz PCIe Gen2 to PCIe Graphics device
A27	LVDS_A0-/eDP_TX0-			B27	PEG_CLK-/RSVD41	
A28	LVDS_A1+/eDP_TX1+	LVDS Channel A differential pair 1 Host data output		B28	LVDS_BKLT_CTRL	Panel Backlight Brightness Control
A29	LVDS_A1-/eDP_TX1-			B29	COM1_DCR	Full RS232 interface from Host to DCE device (shared with back panel COM port and only single may be used)
A30	LVDS_A2+/eDP_TX2+	LVDS Channel A differential pair 2 Host data output		B30	COM1_TX	
A31	LVDS_A2-/eDP_TX2-			B31	COM1_DCD	
A32	GND	Ground connection		B32	GND	Ground connection
A33	LVDS_A3+/eDP_TX3+	LVDS Channel A differential pair 3 Host data output		B33	COM1_DTR	
A34	LVDS_A3-/eDP_TX3-			B34	COM1_RTS	
A35	LVDS_VDD_EN	LVDS Panel Power Enable		B35	COM1_RX	
A36	LVDS_ACLK+/eDP_AUX+	LVDS Channel A differential pair Host clock output		B36	COM1_CTS	Full RS232 interface from Host to DCE device (shared with back panel COM port and only single may be used)
A37	LVDS_ACLK-/eDP_AUX-			B37	COM1_RI	
A38	GND	Ground connection		B38	LVDS_BKLT_EN	LVDS Backlight Enable
A39	LVDS_CTRL_CLK	LVDS Control interface for external SSC clock chip (I2C based). Optional.		B39	LVDS_I2C_CLK	LVDS DDC (I2C based) management interface. EDID support for flat panel display
A40	LVDS_CTRL_DATA			B40	LVDS_I2C_DAT	
A41	PEG_CLK_REQ#/RSVD42	Clock Request Signal for PCIe Graphics (PEG)		B41	GND	Ground connection
A42	RESERVED			B42	RESERVED	
A43	RESERVED	Reserved		B43	RESERVED	Reserved
A44	GND	Ground connection		B44	NC	NC
A45	RESERVED			B45	RESERVED	
A46	RESERVED	Reserved		B46	RESERVED	Reserved
A47	USB_OC_4_5#	USB Overcurrent Indicator for lanes 2/3		B47	SPARE0	Host chipset spare GPIO
A48	USB4_P			B48	VCC_12V	
A49	USB4_N	USB Host interface 4		B49	VCC_12V	
A50	GND	Ground connection		B50	VCC_12V	Main 12V power domain

6.4 Custom Design GPIOs

Intense PC incorporates 7 general purpose input output signals for user application implementations and custom system design. The GPIOs were selected and configured to provide convenient in/out functionality.

Table 32 – Custom Design GPIO table

GPIO	Signal	Direction	Pull (PU/PD)	EXT2 pin#
GPIO6	DGPU_HPD_INTR#	GPI	PU-10k	B16
GPIO17	DGPU_PWROK	GPI/GPO	PD-10k	A10
GPIO50	DGPU_HOLD_RST#	GPO	PU-8.2k	B10
GPIO52	DGPU_SELECT#	GPO	PU-8.2k	A16
GPIO53	DGPU_PWM_SELECT#	GPO	No Pull	A22
GPIO54	DGPU_PWR_EN#	GPO	PU-8.2k	B4
GPIO67	DGPU_PRSNT#	GPI	PU-10k	A4

6.5 Misc Use Connector

Intense PC offers custom use connector with the following connectivity options:

Table 33 – Misc Use Connector

Pin #	Signal	Source Direction	Description
1	5V	Out	5V power
2	IR_OUT	In	IR sensor output
3	3.3V	Out	3.3V power
4	BOARD_LED#	-	Board LED cathode (for external control)
5	SATA_LED#	-	SATA LED cathode (for external control)
6	GND	-	Ground
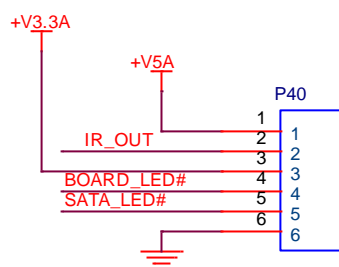
Conn., W2B, Header, 1x6, 1mm, RA, SMT

7 Advanced Technologies

7.1 Intel vPRO technology

Intense PC features Intel vPRO technology in selected models featuring Intel Core i7 processor, QM77 chipset

An added layer of security for businesses and intelligent systems today's businesses and intelligent systems developers face four critical areas of IT security:

- Threat management, including protection from rootkits, viruses, and malware
- Identity and website access point protection
- Confidential personal and business data protection
- Remote and local monitoring, remediation, and repair of PCs and workstations

Intel® vPro™ technology addresses each of these and other needs through its comprehensive set of security, manageability, and productivity-enhancing capabilities. This technology is built into the new Intel® Core™ vPro™ processor family, Intel® chipsets, and network adapters that simplify and accelerate these four critical IT functions.

7.2 Intel Active Management Technology

Intel AMT is a fundamental component of Intel® vPro™ technology. AMT is a set of advanced manageability features developed to meet the evolving demands placed on IT to manage a network infrastructure. Intel AMT reduces the Total Cost of Ownership (TCO) for IT management through features such as asset tracking, remote manageability, and robust policy based security, resulting in fewer desk-side visits and reduced incident support durations. Intel AMT extends the manageability capability for IT through Out Of Band (OOB), allowing asset information, remote diagnostics, recovery, and contain capabilities to be available on client systems even when they are in a low power, or "off" state, or in situations when the operating system is hung.

Intel AMT8.0 technology supported on selected platforms with the following components only and with relevant BIOS support: Intel Core i7 processor, Intel QM77 PCH, Intel GbE MAC/PHY.

7.3 Intel Virtualization Technology

Increasing manageability, security, and flexibility in IT environments, virtualization technologies like hardware-assisted Intel® Virtualization Technology (Intel® VT) combined with software-based virtualization solutions provide maximum system utilization by consolidating multiple environments into a single server or PC. By abstracting the software away from the underlying hardware, a world of new usage models opens up that reduce costs, increase management efficiency, strengthen security, while making your computing infrastructure more resilient in the event of a disaster.

Intel Virtualization Technology (Intel VT) makes a single system appear as multiple independent systems to software. This allows multiple, independent operating systems to run simultaneously on a single system. Intel VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets. Intel Virtualization Technology for IA-32, Intel64 and Intel Architecture (Intel® VT-x) added hardware support in the

processor to improve the virtualization performance and robustness. Intel Virtualization Technology for Directed I/O adds chipset hardware implementation to support and improve I/O virtualization performance and robustness.

8 Power Management

8.1 Power Manager Renesas H8S/2117

Renesas H8S/2117 power manager is an integral part and its HW/FW fully defined by Intel platform architecture. The power manager is a core component in the system and responsible for power management and housekeeping functionality in the platform. It interfaces with processor, chipset, boot devices, system power supplies and power sequencing logic. It is essential part for proper system operation.

The core of H8S/2117 Group of CISC (complex instruction set computer) microcomputers is an H8S/2600 CPU, which has an internal 16-bit architecture.

Figure 15 – Renesas H8S/2117 Functional Block Diagram
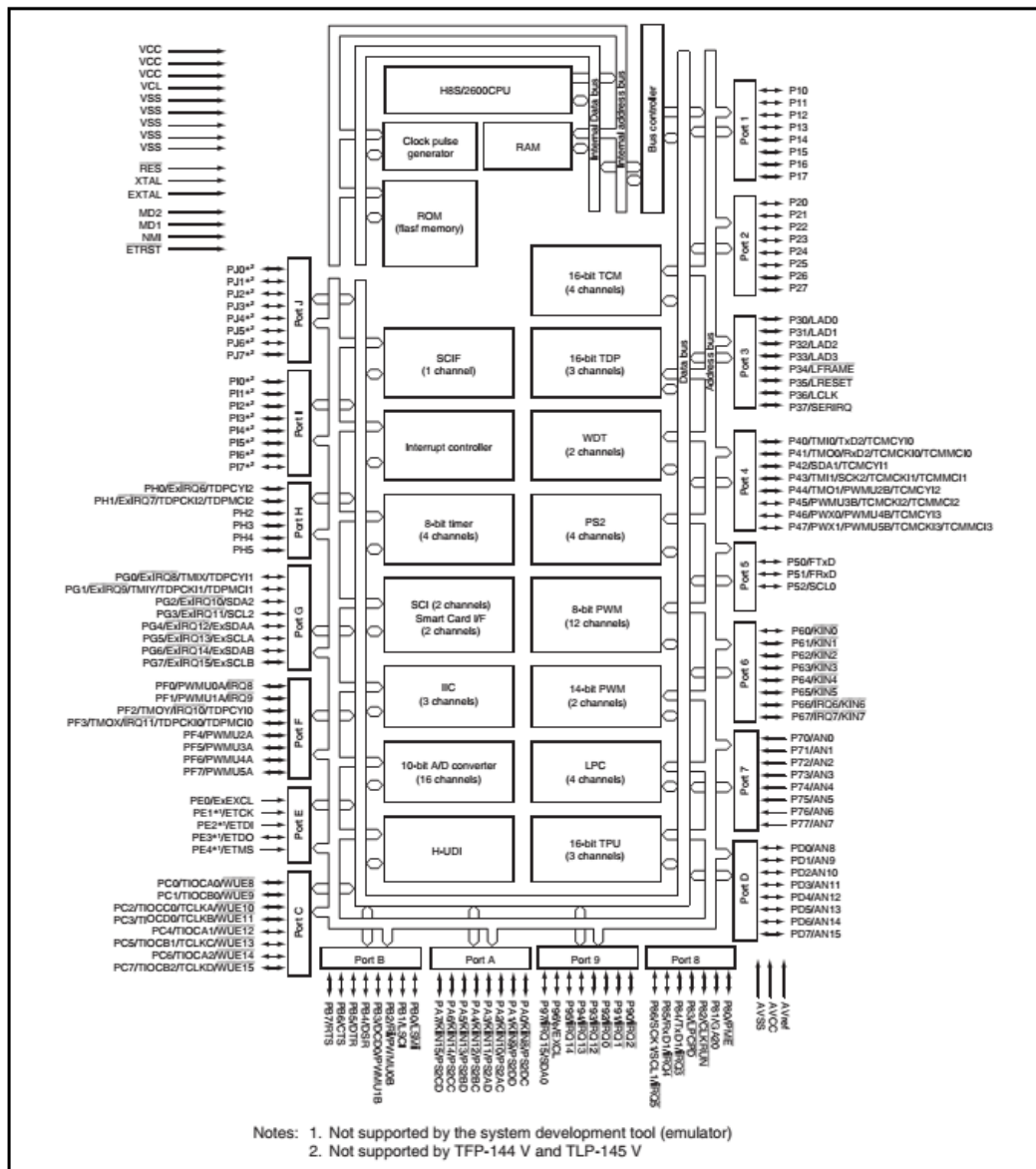
9 Electrical Characteristics

9.1 Absolute Maximum Ratings

Operating the Intense PC under conditions beyond its absolute maximum ratings may damage the device. Absolute maximum ratings are limiting values to be considered individually when all other parameters are within their specified operating ranges. Functional operation and specification compliance under any absolute maximum condition, or after exposure to any of these conditions, are not guaranteed or implied. Exposure may affect device reliability.

Table 34 – Absolute Maximum Ratings

Parameter	Min	Typ.	Max	Unit
Main power supply voltage	8.5	-	16	V

9.2 Recommended Operating Conditions

Operating conditions include parameters that are under the control of the user: power-supply voltage and ambient temperature. The Intense PC meets all performance specifications when used within the recommended operating conditions, unless otherwise noted.

Table 35 – Recommended Operating Condition

Parameter	Min	Typ.	Max	Unit
Main power supply voltage	10	12	15	V

9.3 DC Electrical Characteristics

Table 36 – DC Electrical Characteristics

Parameter	Operating Conditions	Min	Typ.	Max	Unit
		3.3V Digital I/O			
V_{IH1}	GPIO[54, 52, 50, 5:2]	0.5*3.3	-	V5ref+0.5	V
V_{IL1}		-0.5	-	0.3*3.3	V
V_{OH1}		V_PROC_IO - 0.3	-	V_PROC_IO	V
V_{OL1}		0	-	0.255	V
V_{IH3}	GPIO[71:61, 57, 48,	2	-	3.3+0.5	V
V_{IL3}	39, 38, 34, 31:29, 24,	-0.5	-	0.8	V
V_{OH3}	22, 17, 7, 6, 1]	3.3-0.5	-	-	V
V_{OL3}		0	-	0.4	V
V_{IH4}	GPIO[73, 72, 59, 56,	0.5*3.3	-	3.3+0.5	V
V_{IL4}	55, 53, 51, 49, 47:40,	-0.5	-	0.3*3.3	V
V_{OH4}	37:35, 33, 28:25, 23,	3.3-0.5	-	3.3	V
V_{OL4}	21:18, 16:14, 10:8, 0]	-	-	0.4	V

RS232					
TX Voltage Swing		±5.0	±5.4	-	V
Input Voltage Range		-25	-	25	V

9.4 Power Supply

Intense PC wall power supply:

- Input: 100-240VAC 50/60Hz
- Output: 12VDC 5A, 60W

10 Mechanical Characteristics

10.1 Mechanical Drawings

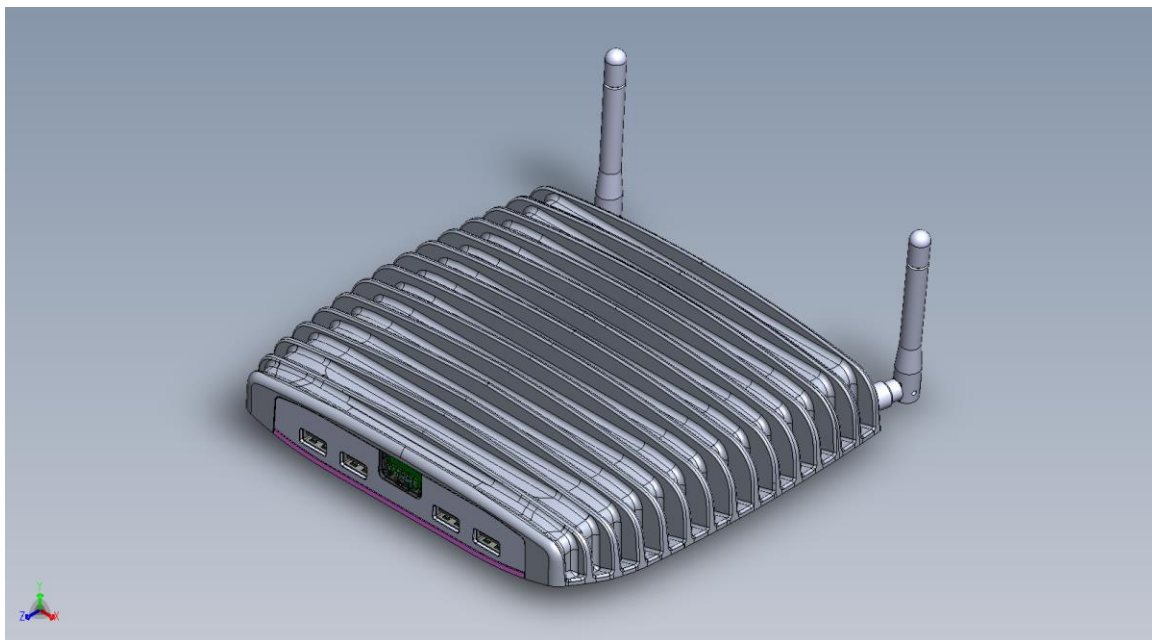### 10.1.1 Chassis

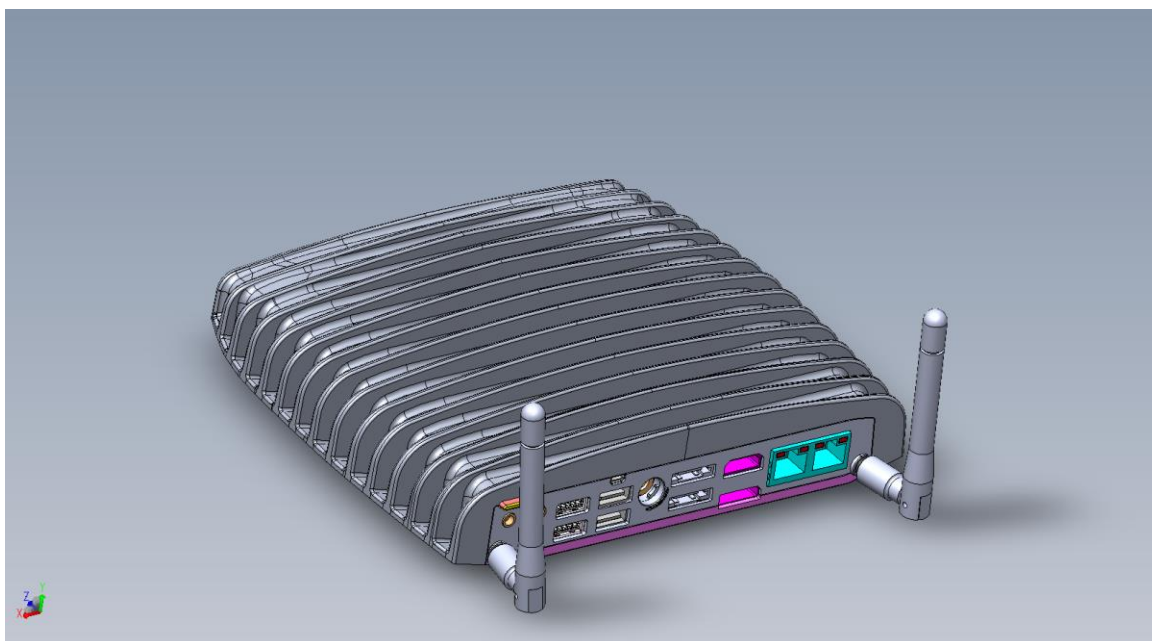**Figure 16 – Intense PC Isometric Front**

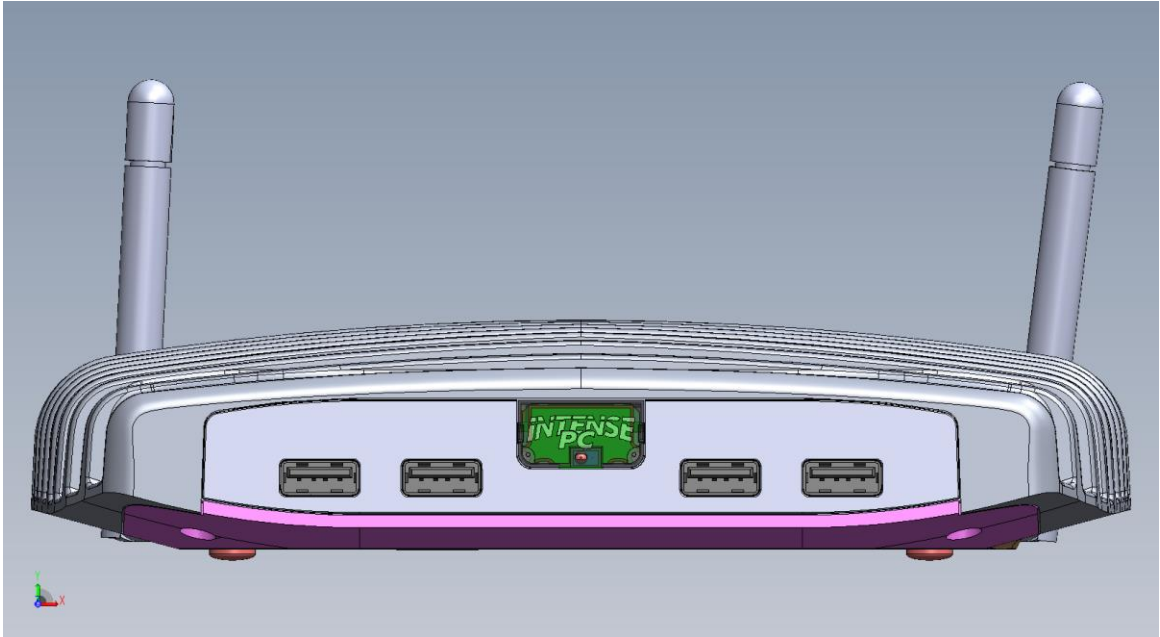**Figure 17 – Intense PC Isometric Back**

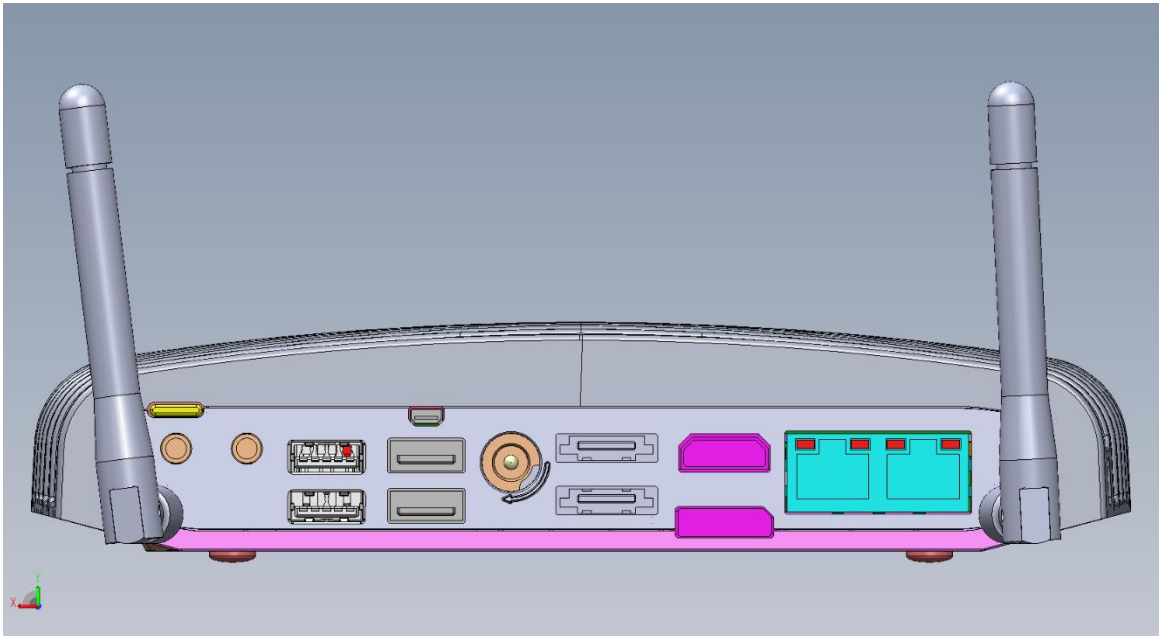**Figure 18 – Intense PC Front Panel**

Figure 19 – Intense PC Back Panel
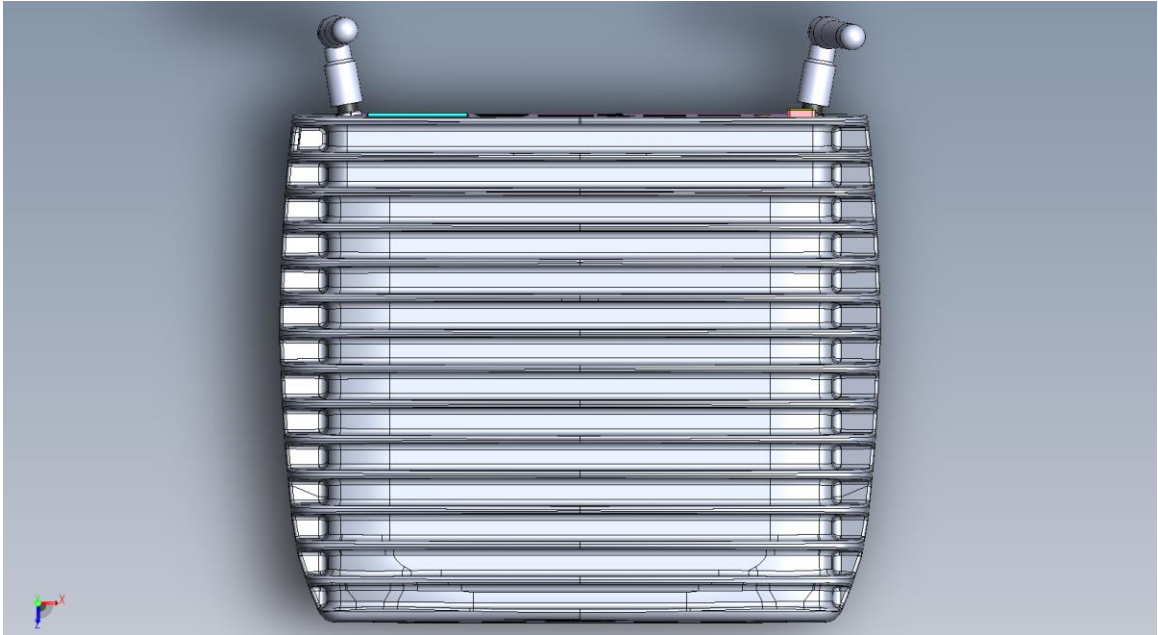
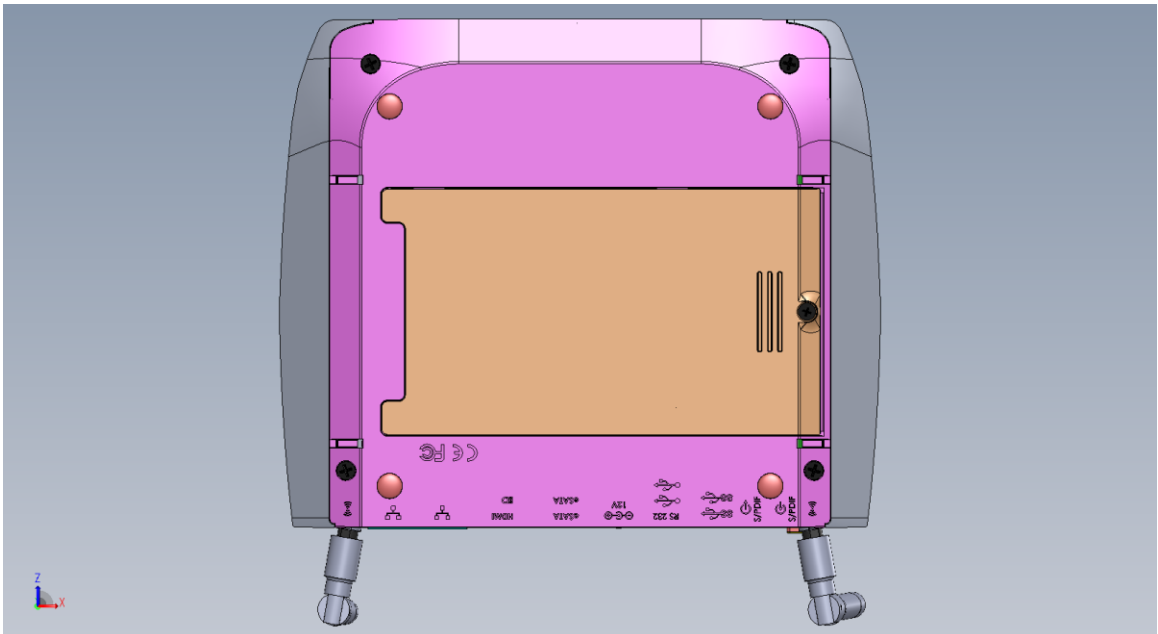**Figure 20 – Intense PC Top**

Figure 21 – Intense PC Bottom

10.1.2 Single Board Computer

Single Board Computers or Open Chassis platforms based on Intense PC HW available for system integration and industrial business applications. Available in both variations with or without FACE Module. SBC HW should be thermally coupled to a passive or active cooling system in order to guarantee proper operation and maximal performance.

SBC supplied with a heat plate in order to simplify system integration and provide an easy way to attach it to a heat sink.
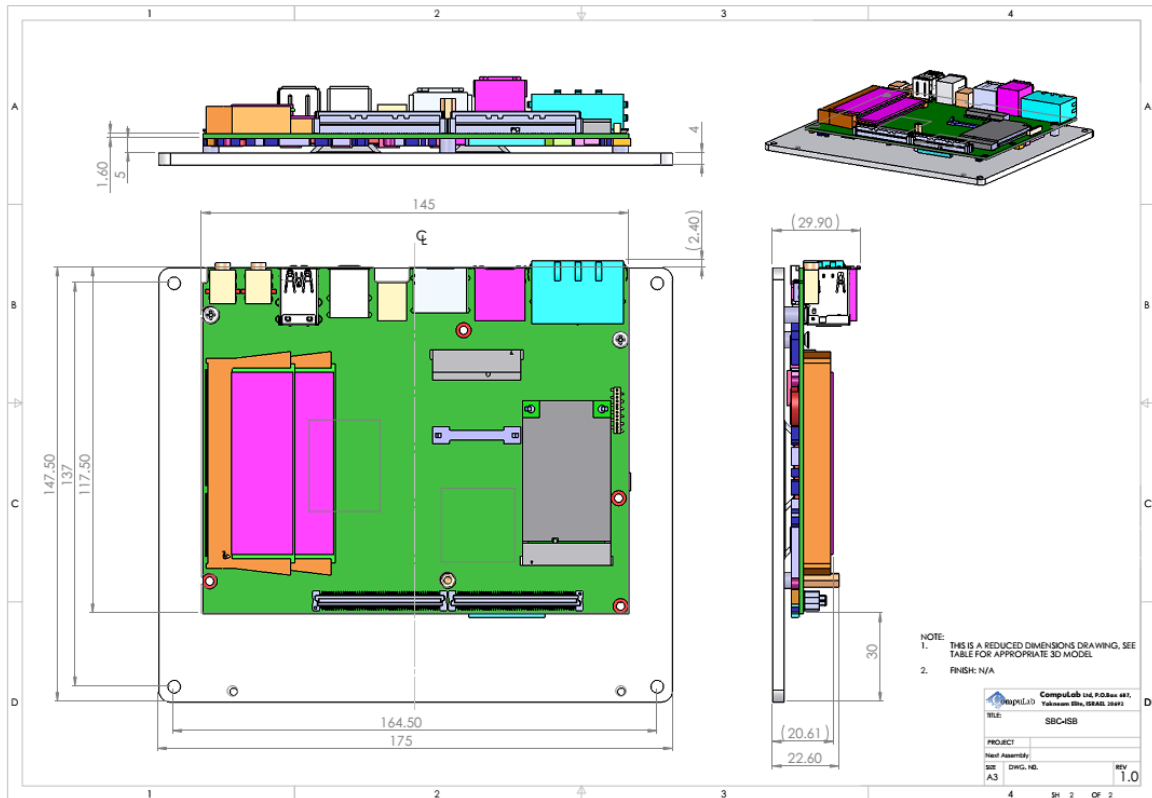
Note: Heat plate alone does NOT guarantee sufficient cooling in order to provide maximal performance, therefore in order to avoid system throttling or thermal shut down in worst cases, system integrators must supply additional system cooling method.

10.1.2.1   With FACE Module

Figure 22 – SBC-iSB Mechanical Drawing with FACE Module
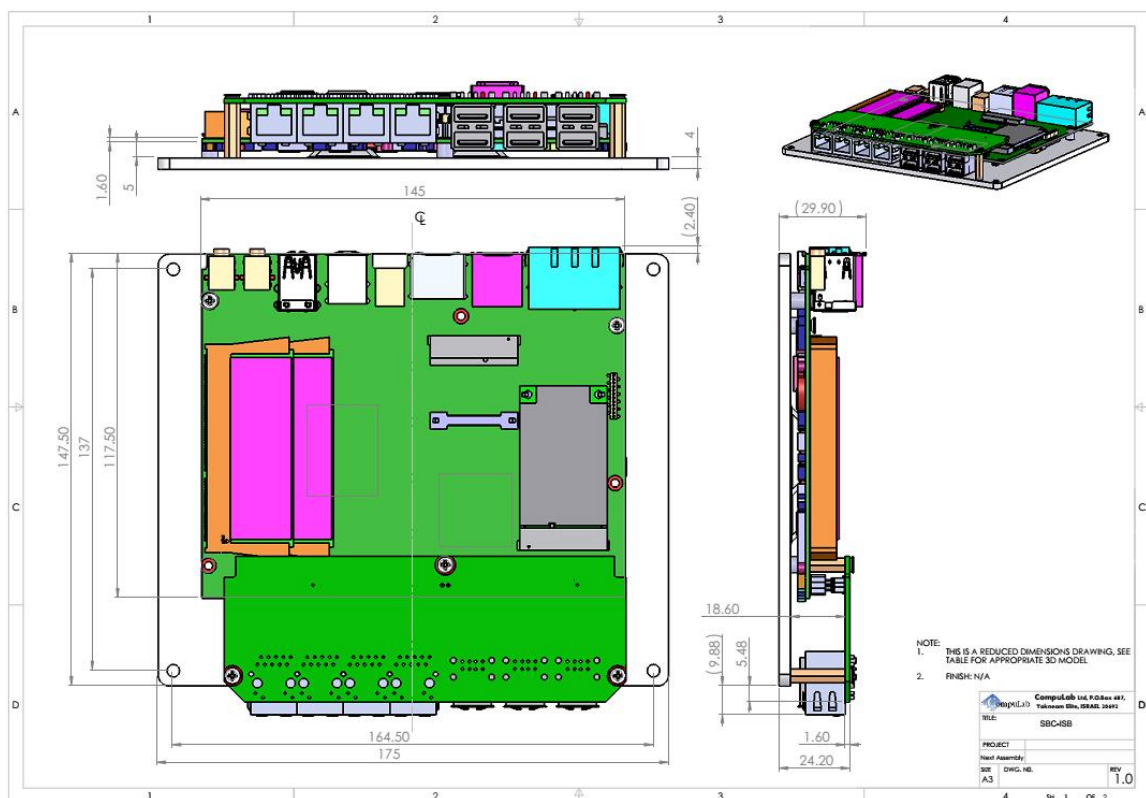
10.1.2.2 Without FACE Module

10.2 Environmental

Intense PC models available in 3 operating temperature grades – Commercial, Extended and Industrial. Please refer to the table below:

Table 37 – Operating Temperature Grades

Operating Conditions	Op. Temp. grades		
	Commercial	Extended (TE)	Industrial (TI)
HDD models	0°C – 50°C	N/A	N/A
SSD models	0°C – 70°C	-20°C – 70°C	-40°C – 70°C

Note: Power supply temperature ratings differs from system ratings, mainly due to material used, and limited to the following:

- Operating: 0°C – 40°C
- Storage: -10°C – 70°C

Customers have the ability to power the computers from another source.

11 Resources

For more Compulab resources please use the following links:

1. Fit-PC website:

    http://www.fit-pc.com/web/

2. Intense PC website:

    http://www.fit-pc.com/web/products/intense-pc/

3. Wiki pages for additional documentation and driver download:

    http://www.fit-pc.com/wiki/index.php/Main_Page

4. Forum:
    http://www.fit-pc.com/forum/index.php?sid=47b935636d5b916b34e9acea453fa815